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BANNING STANDARD CELL ENGINEERING NOTEBOOK

Design Techniques Branch
Electronics and Control Laboratory

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16. ABSTRACT

This notebook describes a family of standardized thick-oxide P-MOS building blocks (standard cells) that are fully compatible with the BANNING Design System and the Computer Aided Design and Test (CADAT) System. The information is presented in a form useful for systems designs, logic design, and the preparation of inputs to both sets of Design Automation programs for array design and analysis. A data sheet is provided for each cell and gives the cell name, the cell number, its logic symbol, Boolean equation, truth table, circuit schematic, circuit composite, input-output capacitances, and revision date. The circuit type file, also given for each cell, together with the logic drawing contained on the data sheet provides all the information required to prepare input data files for the Design Automation Systems. The appendixes contain a detailed description of the electrical design procedure.

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BANNING STANDARD CELL ENGINEERING NOTEBOOK

SECTION I: INTRODUCTION

A. PURPOSE OF THIS NOTEBOOK

This notebook describes a family of standardized thick-oxide P-MOS building blocks fully compatible with the BANNING Design Automation System. These standardized building blocks are the BANNING standard cells. The information in this notebook is presented in a form useful for systems design, logic design, and the preparation of inputs to the BANNING Design Automation programs for array design and analysis.

The Design Automation System consists of five major programs. Two of these programs are used to translate a logic design into precision MOS-FET artwork. These are:

Placement-Routing-Folding (PRF) Program

Artwork Program

The remaining three programs are used to analyze the performance of basic circuits and logic nets. These are:

Logic Block Simulator

Signal-Trace Program

Transient Analysis Program

These programs are discussed briefly in Section I. C.

The standard-cell design-automation approach offers the following advantages when compared with conventional manual techniques:

1. Improved Accuracy

The manual operations now being used for composite drawing and rubylith cutting are completely bypassed when using the automated procedures. These automated design procedures appear at the present time to be the only way to handle these operations with a minimum of human error.

2. Improved Turn-Around Time

Final accurate artwork is available in several days compared to the month or more required for the manual procedure.

3. Elimination of Layout-Rule Violations

Each cell topology is accurately digitized, check-plotted, and committed to the library magnetic-tape storage. Subsequent uses of a given cell are therefore free of human error.

4. Accurate Time Simulation of Each Logic Net of the Total Array

The Signal Trace Program provides a pictorial printout of each net of logic and its branches.

5. Accurate Logic Simulation

Each cell of the library can be logically described by the Logic Block Simulator.

6. Worst-Case Electrical Design

Because a given cell is designed only once, the designer can afford to spend much more time optimizing the electrical design of each cell.

B. ORGANIZATION OF THIS NOTEBOOK

Section II of this notebook contains the electrical specifications for the circuit family, the design rules used to lay out the cells, and the process parameters upon which the circuit design and layout are based. Section III contains the cell-layout topology rules. The inclusion of this data in the notebook provides the user with a better understanding not only of the devices but also the fabrication processes involved and provides sufficient information for the design and layout of special cells or new cells compatible with the family. Section IV furnishes the logic designer with all the cell information required for array design and the compilation of net list data for the Design Automation programs. Section IV. B contains the specification sheet for each BANNING cell (the data sheets). These sheets, one for each cell, provide the cell name,

the cell number, its logic symbol, Boolean equation, truth table, circuit schematic, circuit composite, input-output capacitances, and date of issue. The circuit type file contained in Section IV. C, and a logic drawing provide all the information required to prepare input data files for the Design Automation System. The Appendixes contain a detailed description of the electrical design procedure.

C. BANNING DESIGN AUTOMATION PROGRAMS

1. MOS Logic Block Simulator

This program is a self-contained compiler designed to simulate binary logic systems composed of interconnected MOS-FET standard cells. The input to the simulator is punched cards. Each cell required is described by one card punched to specify cell type, input connections, and other parameters as required. Since the function of each cell is described by an individual subroutine of the Logic Block Simulator, it is necessary for the logic designer to use only those logic blocks contained in the standard circuit library.

The output consists of printed columns containing 1's and 0's representing the output values of specified cells as they exist at the end of a Phase I or Phase II clock time. For a given computer run, the number of cells that may be displayed is limited by the number of columns available on the output printer of the computer, typically 120 columns. Voltage at every node is calculated and can be printed at time increments small enough to display the logical values at the end of every high-speed clock time.

The simulator will accommodate systems as large as 4000 cells and having as many as 100 different standard cell types. These cell types must correspond to the fixed set recognized by the simulator.

2. Placement-Routing-Folding-Program (PRF)

After the logic designer is assured by the simulation program that his logic works, and after the system has been partitioned into individual arrays, the data cards for each chip used for the final simulation are used as input to the PRF program. This

eliminates the need for special data preparation and consequent human error. The input routine of the PRF program automatically converts this data to its own required input format. Depending upon the number of cells to be placed and interconnected, between 5 and 20 minutes of machine running time is required for this program.

The final placement of cells on a chip is decided upon by a computation to establish a suitable minimum total wire-length for intraconnecting the array. Cells are first interchanged until a satisfactory placement is accomplished. Then the interconnections are routed utilizing aluminum metalization and P-diffusion tunnels.

This program provides the following computer printouts to aid the engineer in the total array design:

(a) Two basic categories of capacitance loading information:

(1) Loading before interconnections are routed.

(2) Loading after interconnections are routed.

(b) Folded-array printout showing chip size. Cell locations, cell orientations and type, and paths of all interconnections.

(c) A printout of the predicted speed performance of the array, as determined by the Signal-Trace Program.

(d) A listing of the PRF Program output specifying cell locations and orientations, signal interconnections, and power bus and bonding pad locations. This particular output is available in printed form, on magnetic tape, or on punched cards. All outputs are fully compatible with the Artwork Program.

3. Artwork Program

This program is used to generate the commands for the Gerber Plotter to draw the required artwork for the MOS-FET arrays. The program output tape contains light aperture and motion commands which control the Gerber Plotter. The topology describing

the individual cells is stored on the library tape for the Artwork Program. From the input specifications furnished by the PRF program and the list of apertures available at the plotter and the scale desired for the output artwork, the Artwork Program calculates the Gerber instructions to draw artwork for each level of the MOS-FET chip. There are several options available for drawing the polygons that compose the individual cells. The option providing the highest degree of precision consists of first outlining the polygons using the smallest available light aperture and then filling in the remaining, less critical areas by using larger light apertures, all under program control. Accurate test plots for verification of artwork can be made by outlining only (omitting the "fill" step), thus conserving plotter time. The Artwork Program also provides a number of "housekeeping" functions such as updating the standard cell library tape and formulating Gerber instructions for drawing standard cell composites from the digitized cell data.

4. Signal-Trace Program

This program is designed to run as a subroutine of the PRF program. With this program, a highly accurate time analysis prediction for the complex MOS-FET array is possible. The basic logic structure for two-phase four-delay logic circuits is described as functions that originate at the output of a terminal-type element and end at another terminal-type element after propagating through as many as four levels of gating or combinatorial type logic. The program searches for the elements that constitute terminal elements; a logic tree composed of terminal-type elements separated by logic gates is described. The Signal-Trace Program first identifies every branch of the various logic trees and predicts the time response of that branch for two conditions of operation: 1) the time required for a beginning terminal element to change from a logic "1" to a logic "0", and 2) the time then required for the opposite transition at the beginning terminal. The Signal-Trace Program uses the capacitance loading figures calculated by the PRF Program to assess the time response of each node within the branch.

5. Transient Analysis Program

This program is used to evaluate the response times of the basic BANNING cells. The three cells of the family, which serve as cells and also as component parts of more complex cells, are 1) the inverter, 2) the inverter with delay, and 3) the NAND gate. The program input comprises the Sah Model equations and device parameters. The program output is a printout of the nodal voltage versus time. The Sah Model and the derivation of equations is given in Appendix A of the notebook.

Section II

CELL DESIGN PARAMETERS

This section comprises two tables that list the basic electrical and process parameter specifications for the cell family. The cell designs given in this notebook are valid for the two thick-oxide processes now being used by several fabricators. The depth of p-diffusion in the shallow diffusion process is less than 0.07 mil; in the deep diffusion process, the diffusion is greater than 0.1 mil.

Table I lists the basic electrical specifications for the cell family. These parameters are valid for both processes. Under rated load conditions, the cells must be capable of propagating a signal through four levels of combinatorial logic for worst-case conditions during one clock time at a maximum clock rate of 850 kHz. The only restriction on worst-case conditions is that voltages may not vary in opposite extremes; for example, V_{DD} cannot be maximum while V_{GG} is minimum.

Table II lists the process parameters that are not process dependent. These are the resistance per square, the capacitive coefficients of the various regions per square mil, and the mask alignment. The K' parameter and the lateral p-diffusion depths are different for the two processes now in use and are presented in Table III.

TABLE I. ELECTRICAL SPECIFICATIONS

ELECTRICAL PARAMETER	PERMISSIBLE VALUES
V_{DD}	-13.3 to -15.3 V
V_{GG}	-23.8 to -27.4 V
V_T	-3.5 to -4.5 V
Clock Frequency (Max)	850 kHz
Ambient Temperature	-55 to +125°C

TABLE II. STANDARD PROCESS PARAMETERS (FOR BOTH PROCESSES)

PROCESS PARAMETER	PERMISSIBLE VALUE
R_{pN}	150 Ω per square (resistance of p-region)
C_{pN}	0.07 pF/mil^2 (p-region to substrate)
C_{MF}	0.02 pF/mil^2 (metal over thick oxide)
C_{MG}	0.2 pF/mil^2 (metal over thin oxide)

Mask Alignment Tolerance is 0.1 mil

$K' \propto T^{-3/2}$

V_T (effective) $\propto$ V_T(nominal) + $\frac{1}{2}\sqrt{V_{BS}}$

TABLE III. PROCESS-DEPENDENT PARAMETERS

PROCESS PARAMETER	DEEP DIFFUSION PROCESS	SHALLOW-DIFFUSION PROCESS
Lateral p-diffusion depth	0.12 mil	0.05 mil
K'_{25} (K' at 25°C)	1.8 to 2.2	3.0 to 4.0
K'_{-55} (Max)	3.51	6.38
K'_{135} (Min)	1.12	1.86

Section III

CELL AND ARRAY LAYOUT RULES

This section presents the rules governing cell and array layout. Metal, p-material, gate oxide, and cutout sizes and relative minimum spacings are given. Configuration drawings of the three types of active devices — the clock gate or coupling gate, the load element, and the inverter (transistor) gate — are included together with tables listing their properties such as lengths, widths, and area overlaps.

Other rules are listed which pertain only to the array level of layout include pad size and spacing, border width and spacing, pad-to-border and pad-to-metalization spacing, etc. All dimensions are given in mils except where otherwise specified.

A. MINIMUM DIMENSIONS

Figure 1 shows the minimum dimensions for the thick-oxide standard cells. All dimensions are given in mils.

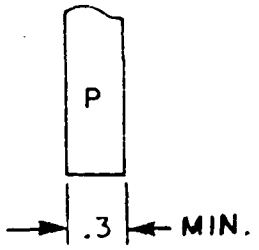
B. MINIMUM SPACING

Figure 2 shows the minimum spacing permitted for cell layout. Figure 3 shows the p-to-p spacing for cells in adjacent rows. All dimensions are given in mils.

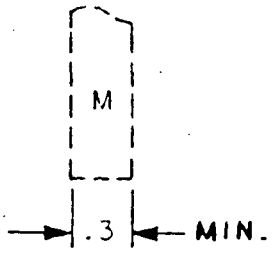
C. ACTIVE-DEVICE-AREA OVERLAPS

1. Load Devices

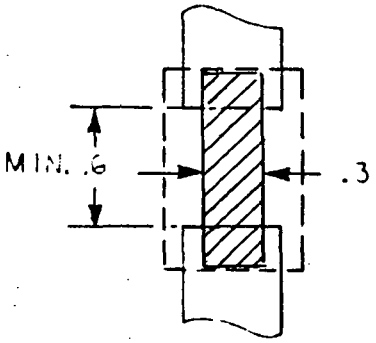
Figure 4 shows the permissible overlaps for the load devices. All dimensions are given in mils.



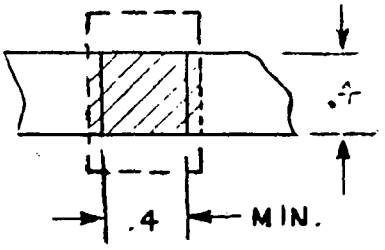
(a) P-Material: 0.3 width



(b) Metal: 0.3 width

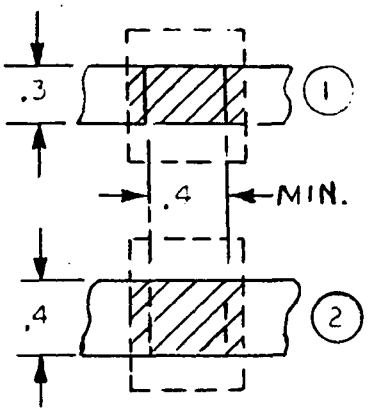


(c.1) 0.3 width, 0.6 length

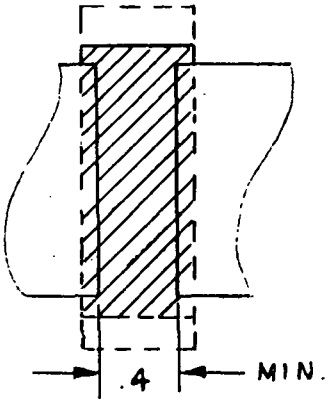


Load devices.

(c.2) 0.4 width, 0.4 length



(d) Coupling transmission device

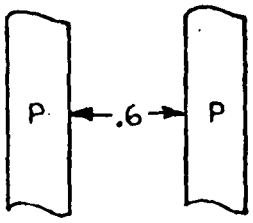


(e) Inverter device; 0.4 length

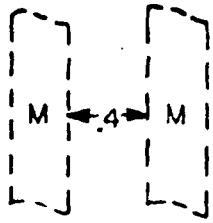
(1) Internal to cell: 0.3 width, 0.4 length

(2) External to cell: 0.4 width, 0.4 length

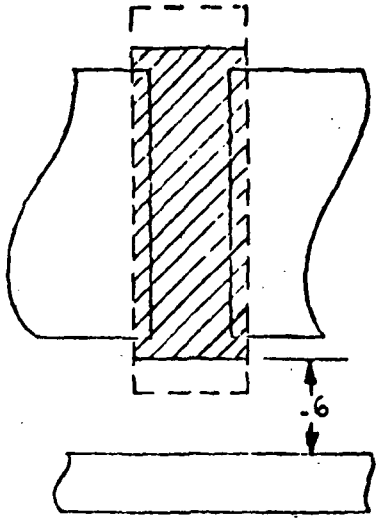
Fig. 1. Minimum dimensions for cell layout.



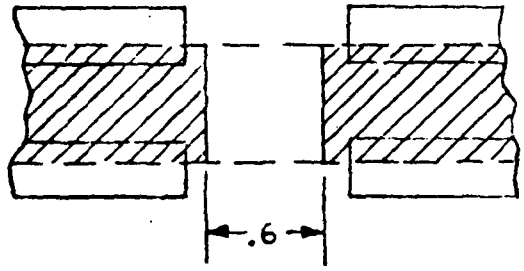
(a) P-to-P spacing: 0.6



(b) Metal-to-metal: 0.4

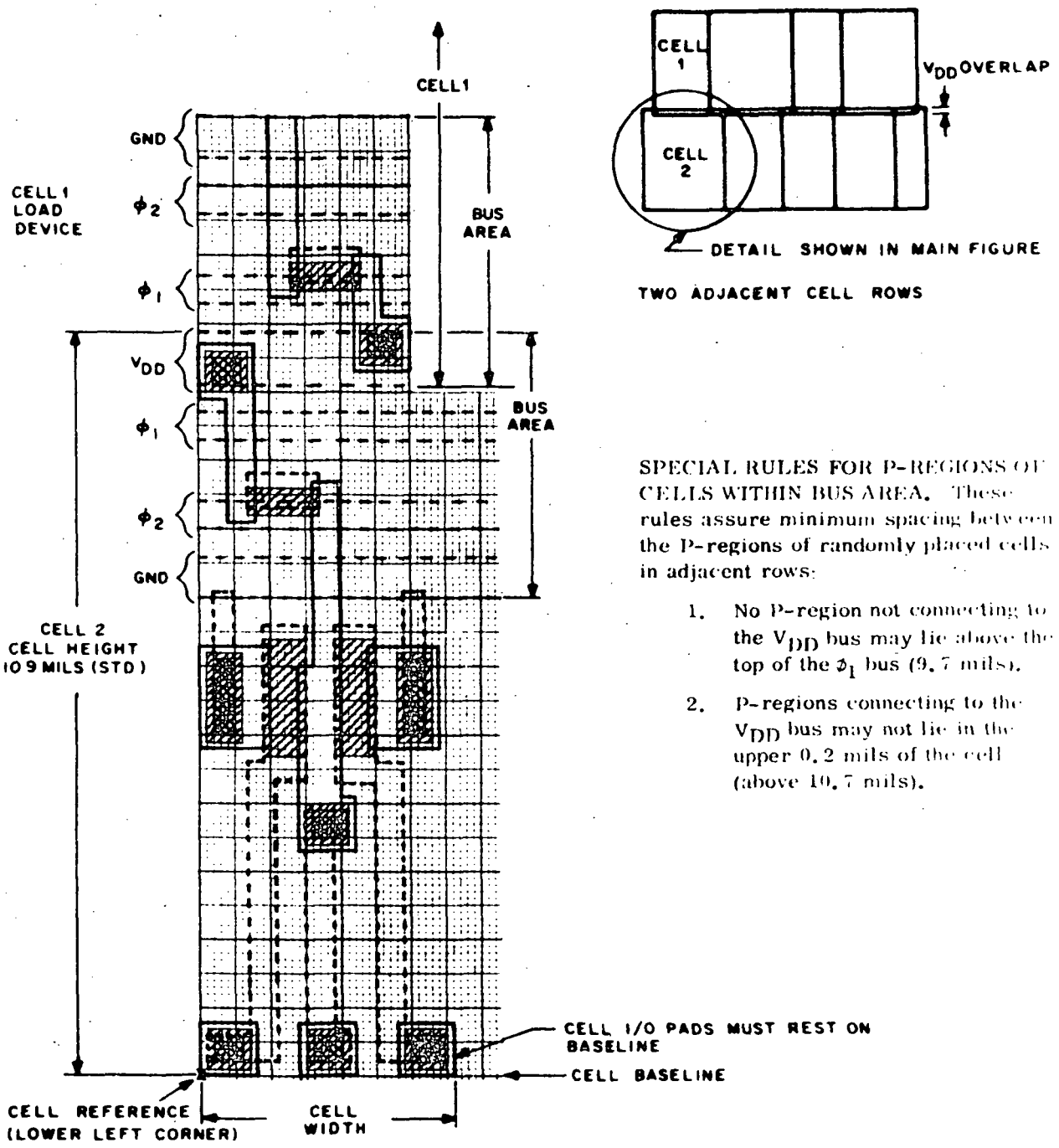


(c) Gate oxide to adjacent P: 0.6



(d) Oxide-to-oxide: 0.6
Load-coupling devices having the same clock may have a common oxide.

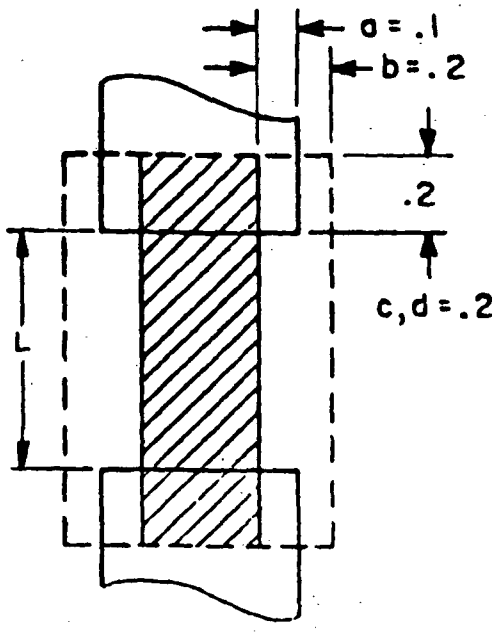
Fig. 2. Minimum spacings for cell layout.



SPECIAL RULES FOR P-REGIONS OF CELLS WITHIN BUS AREA. These rules assure minimum spacing between the P-regions of randomly placed cells in adjacent rows:

1. No P-region not connecting to the V_{DD} bus may lie above the top of the ϕ_1 bus (9.7 mils).
2. P-regions connecting to the V_{DD} bus may not lie in the upper 0.2 mils of the cell (above 10.7 mils).

Fig. 3. P-to-P spacing for cells in adjacent rows.



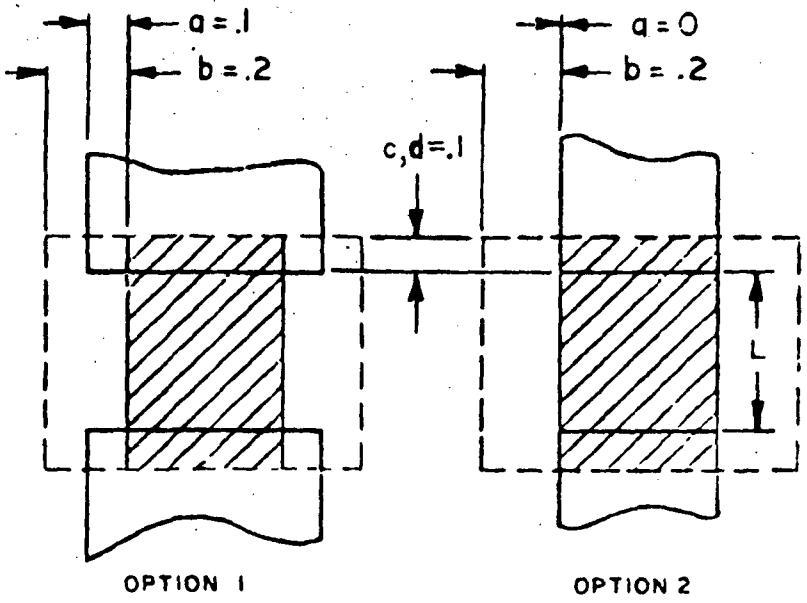
(a) 0.3-mil-wide element.

Width Direction

a. P-beyond gate oxide: 0.1
b. Metal beyond gate oxide: 0.2

Length Direction

c. Gate oxide beyond P edge: 0.2
d. Metal beyond P edge: 0.2



(b) ≥0.4-mil-wide element.

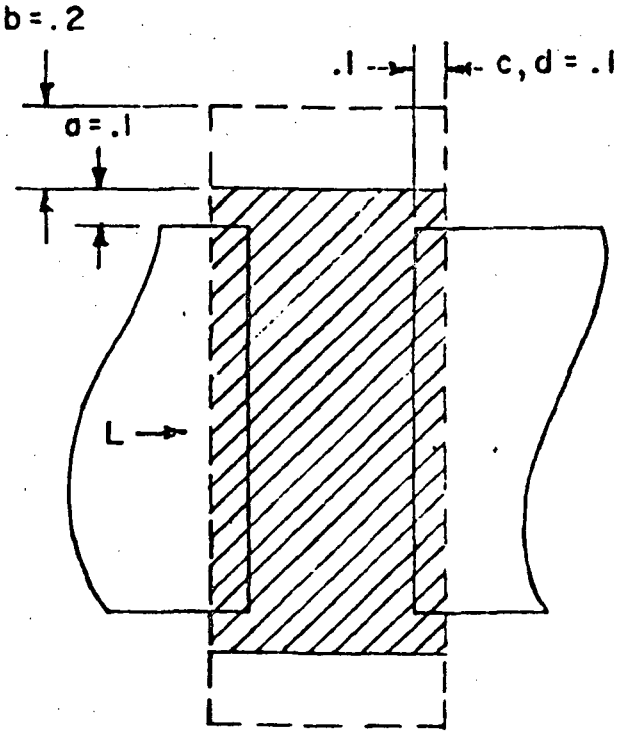
	Option 1	Option 2
Width Direction		
a. P beyond gate oxide	0.1	0
b. Metal beyond gate oxide	0.2	0.2
Length Direction		
c. Gate oxide beyond P edge	0.1	0.1
d. Metal beyond P edge	0.1	0.1

Note: When L < 0.6, use Option 2

Fig. 4. Permissible load-device area overlap.

2. Inverter Devices

Figure 5 shows the permissible overlaps for the inverter devices. All dimensions are given in mils.



Width Direction

a. Gate oxide beyond P: 0.1
b. Metal beyond gate oxide: 0.2

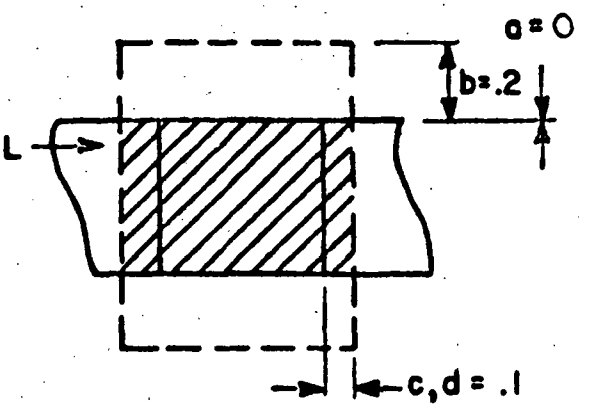
Length Direction

c. Gate oxide beyond P edge: 0.1
d. Metal beyond P edge: 0.1

Fig. 5. Permissible inverter-device area overlap.

3. Coupling Device

Figure 6 shows the permissible overlaps for the coupling device. All dimensions are given in mils.



Width Direction

a. P beyond gate oxide: 0.0
b. Metal beyond gate oxide: 0.2

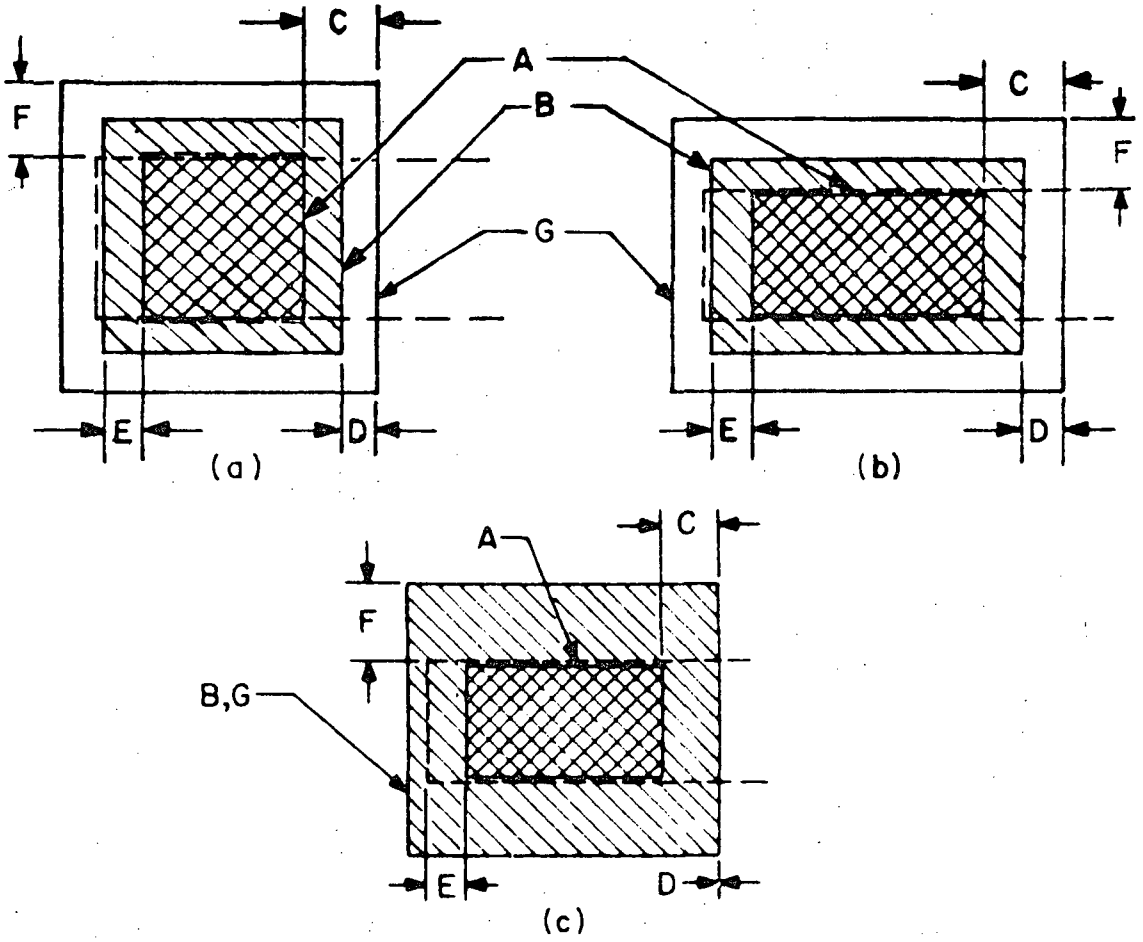
Length Direction

c. Gate oxide beyond P edge: 0.1
d. Metal beyond P edge: 0.1

Fig. 6. Permissible coupling-device-area overlap.

D. CONTACT DIMENSIONS

Figure 7 shows the minimum contact dimensions, all of which are given in mils.



Note: Actual contact area is cross-hatched.

A.	2nd mask, minimum dimensions:	0.4 x 0.4	0.3 x 0.6	0.3 x 0.5
B.	3rd mask, minimum dimensions:	0.6 x 0.6	0.5 x 0.8	0.7 x 0.
C.	2nd mask to edge P-region.	0.2	0.2	0.1
D.	3rd mask to edge P-region.	0.1	0.1	0
E.	2nd-mask — metal overlap in direction of travel or in instances where no area penalty occurs	0.1	0.1	0.1
F.	2nd mask to edge P-region vertical direction	0.2	0.2	0.2
G.	minimum dimension 1st mask	0.8 x 0.8	0.7 x 1.0	0.7 x 0.8

Fig. 7. Contact dimensions.

E. OVERALL CELL DIMENSIONS

None of the lines shown in Fig. 8 are part of a cell layout. They are being used in the figure to represent a typical cell area and the associated bus structure. In particular, it should be stressed that the bus structure, although shown here and on each data sheet composite, is not part of the digitized cell information. It is generated automatically by the BANNING D/A Programs when a chip is made.

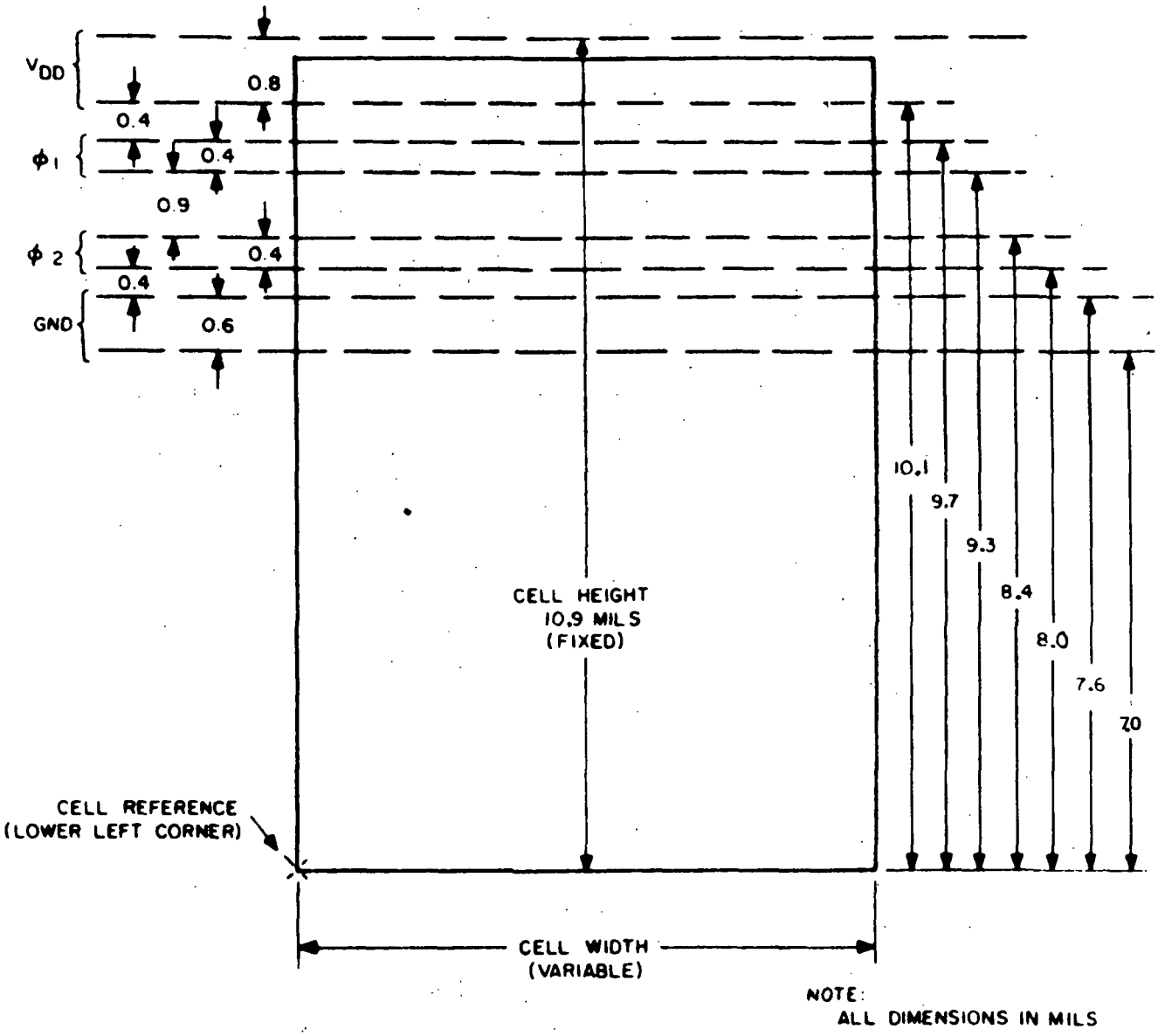


Fig. 8. Overall cell dimensions.

F. ARRAY COMPONENT DIMENSIONS AND SPACINGS

Table IV contains the dimensions for the components and spacings on the array.

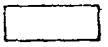
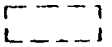
TABLE IV. COMPONENT DIMENSIONS AND SPACINGS

COMPONENT OR SPACING	SIZE (MILS)
P to edge of scribe area	1.6
Scribe-area edge to center	2.0
Scribe-area width on one level	3.0
Pad to circuit metal	1.6
Metal-to-scribe area edge	1.6
Pad size	4.0 x 4.0
Pad-edge to pad-edge spacing, minimum	3.0
Pad to scribe-area	2.0
Pad to scribe-line	4.0
4th mask border which circumscribes other borders	3.0

G. SYMBOLISM FOR COMPOSITE MASKS

Table V shows the symbolism for each of the four required masks.

TABLE V. MASK SYMBOLISM

MASK		COMPOSITE SYMBOLISM
No.	Description	
1	P-mask	
2	1st-contact hole and gate oxide-removal mask	
3	2nd-contact hole mask	
4	Metal mask	

Section IV

DATA SHEETS

A. DISCUSSION OF DATA SHEET PARAMETERS

1. General Discussion

This section contains a set of data sheets describing each cell of the BANNING thick-oxide P-MOS cell family. In those cases where two cells are identical except for the clock phase of the load device (or transmission gate), both cells are documented on one data sheet. Each data sheet provides the logic designer with all the cell data required to design and draft a complex digital equipment comprised of BANNING cells. The relevant data for the logic designer are:

Cell name, number, drive capability, and output clock phase

Truth table

Logic Symbol (s) with I/O pin numbers

Logic Equation (s)

The data sheets also contain a circuit schematic, an I/O pin capacity table and a composite of the cell layout.

In general, four levels of combinatorial logic may be used on one clock phase. Exceptions to this rule, primarily static register inputs, are noted on the individual data sheets. The maximum clock repetition rate for four-level logic is 850 kHz. The clocks are nonoverlapping with a dwell time between clocks of about 70 nanoseconds. Thus, each clock pulse is equal to V_{GG} for 525 nanoseconds.

The cell information required for array design or logic simulation (but not requiring the data sheets as reference) has been placed in a separate subsection following the data sheets. This subsection contains the circuit-type file and a table of cell widths. The former provides input-output pin spacings, capacitance, and the reassignment flags that are necessary to prepare the data input files for the BANNING PRF Program and for logic simulation.

2. Common Data

Table VI contains data pertaining to all the members of the BANNING cell family. This data is therefore not included on each data sheet.

TABLE VI. DATA COMMON TO ALL CELLS

PARAMETER	SYMBOL	MIN	MAX
Power Supply	V_{DD}	-13.3	-15.5
Clock Voltage	V_{GG}	-23.8	-27.4
Threshold Voltage	V_T	- 3.5	- 4.5
Ambient Temperature	T_{AMB}	-55°C	+125°C
Clock Frequency		---	850 kHz

Process and topology parameters, such as material capacitance coefficients, depth of diffusion, mask alignment tolerance, etc., are contained in Section II.

3. Data Sheet Details

a. Front of Data Sheet

The front of each data sheet contains the cell name and number, date of issue, schematic, logic symbol, truth-table, logic equation(s), and an input-output pin-capacity table. In the schematic drawing, input and output lead ends are circled; bus connections, clocks, and dc power are not. On single-cell data sheets, the clock phase symbols ϕ_1 and ϕ_2 are used in the schematic, truth table, and the logic symbol. On twin-cell data sheets, the clocks on the schematic, logic symbol and truth table are indicated symbolically by ϕ_W and ϕ_X. In these cases, the proper clock phase is indicated parenthetically beside the cell number. For example, the first data sheet is for cells 2070 and 2080, whose Cell Numbers are given as:

2070 (ϕ_1)

2080 (ϕ_2)

The cell drive capability is indicated parenthetically beside the cell name. Using the same cell as an example,

TWO-INPUT NOR, 2 pF

Cell inputs are labeled A, B, C, D...., N. The one exception is that the trigger input of the BINARY uses the letter T. Cell outputs are labeled P and S for the primary and secondary outputs. Cell input and output pin numbers are given external to the logic symbol. Letters and numbers are also contained within the symbol to further identify the pin; examples are R and S used to designate reset and set inputs of flip-flops, and One and Zero on the outputs. Likewise, C and $\overline{C}$ are used to identify the carry and carry-not outputs of the BINARY.

In the truth tables and logic equation blocks, the subscript t-1, as in A_{t-1} and P_{t-1}, refers to A and P at the time prior to the indicated clock, this is not necessarily the previous clock phase since the clocks must not overlap. The set and reset inputs to registers are also mutually exclusive.

In the I/O pin capacity block, capacity is given in femtofarads (fF). One femtofarad is equal to 10^{-15} Farads.

b. Back of Data Sheet

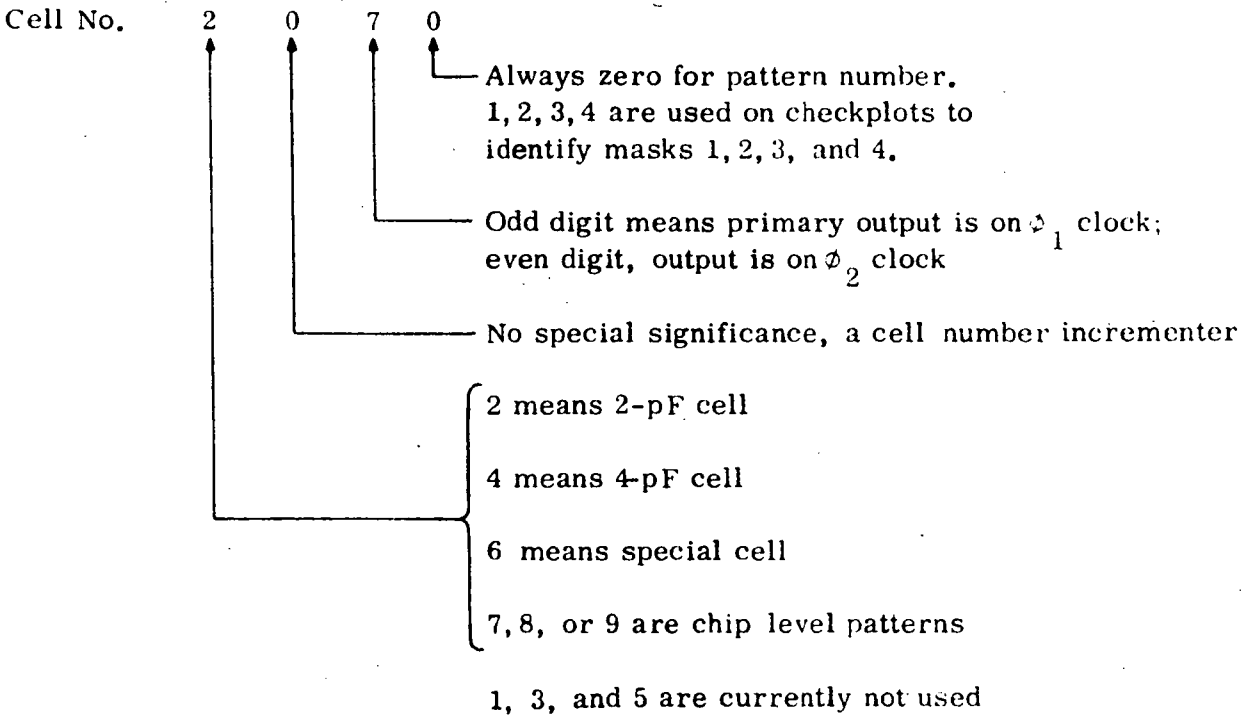
The reverse side of each data sheet contains a scaled composite layout of the cell(s) described on the front side. Each large division equals one mil (10^{-3} inches), and each small division equals one-tenth mil. The different areas or mask levels are denoted as shown in Table V. Double cross-hatched regions represent areas where levels 2 and 3 overlap; these are the contact areas. Power and clock buses shown on the composite are not part of the cell pattern and are included for reference purposes only. The bus structure, including the chip power pads, is generated by the BANNING Design Automation programs. Note that the primary and secondary outputs on the composite are called Q and $\overline{Q}$, respectively.

c. Cell Number Significance

Cell Numbers 2000 to 2990 are used and reserved for cells that have an output drive capability of 2 pF, cell numbers 4000 to 4990 are reserved for cells with an output drive capability of 4 pF. The 6000-series cells include special-function and

high-drive-capacity cells such as transmission (clock) gates, 10 pF inverters, line drivers, and super-cell subunits. The load capacity of each cell is indicated parenthetically beside the cell name on each data sheet. The 7000-, 8000-, and 9000-series numbers are reserved for patterns used only at the chip level of BANNING design: such as chip input/output and power pads, chip border, alignment keys, test transistor pattern, etc.

The significance of various digits of the cell number are shown below. Cell Number 2070 is used as an example of a typical cell number.



d. Special Cell Considerations

1.) General

The general description of each cell contains the Boolean function and the truth table for that cell. In some cases the truth table is not complete due to the many possible input conditions. In other cases, an asterisk (*) is used to indicate that

the value of a given input (one or zero) does not affect the given output condition. In each case, however, a representative truth table is given. If two inputs have the same effect on the output, only one may be shown or the Boolean equivalent of both inputs. Each cell number and name is given, as well as the Mil Logic form. In order to avoid confusion about which cell is being described a more detailed Mil Logic form is given for cells normally represented by a block, e.g., the static register. Transients and their causes are discussed in this section and in Appendix A. Waveforms are given in Figs. 9 to 14 inclusive.

e. Logic Element Characteristics

1.) Inverter and NOR Gates Without Delay

As shown in the truth table for gates of this type, the output is not necessarily the inverse of the input. The output of inverter (or gate) with a clocked load can go to ground on either clock time, which means it directly follows the input Zero-One transition. This is not true when the input makes the One-Zero transition. The output must wait for the following clock to turn on the load device if the input transition from One-Zero is on the opposite clock time. If, however, the One-Zero transition occurs on the clock time which operates the load device, the output will follow the input.

If two gates in series have the same clock operating their loads, the output of the second will always change during that clock time, no matter when the input transition occurs. If the input transition occurs on the opposite clock there will be 1/2-bit of delay through the two stages.

2.) Inverter and NOR Gates with Delay

The output of this type of gate will always change on the clock time which operates the load device. If the input is at the same clock time as the load device there will be no delay. If the input is at the opposite clock time there will always be a 1/2-bit of delay.

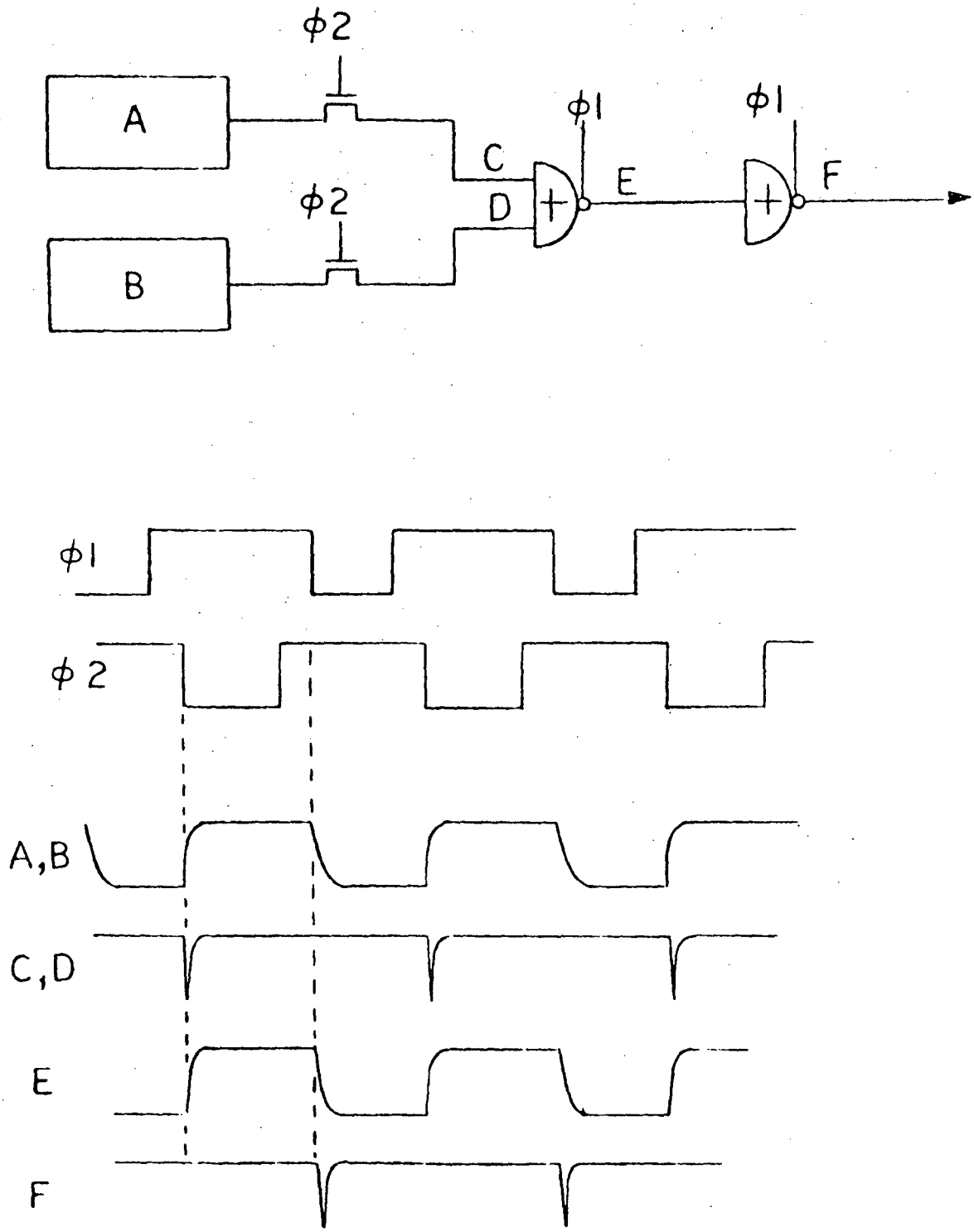


Fig. 9. Precharge transient.

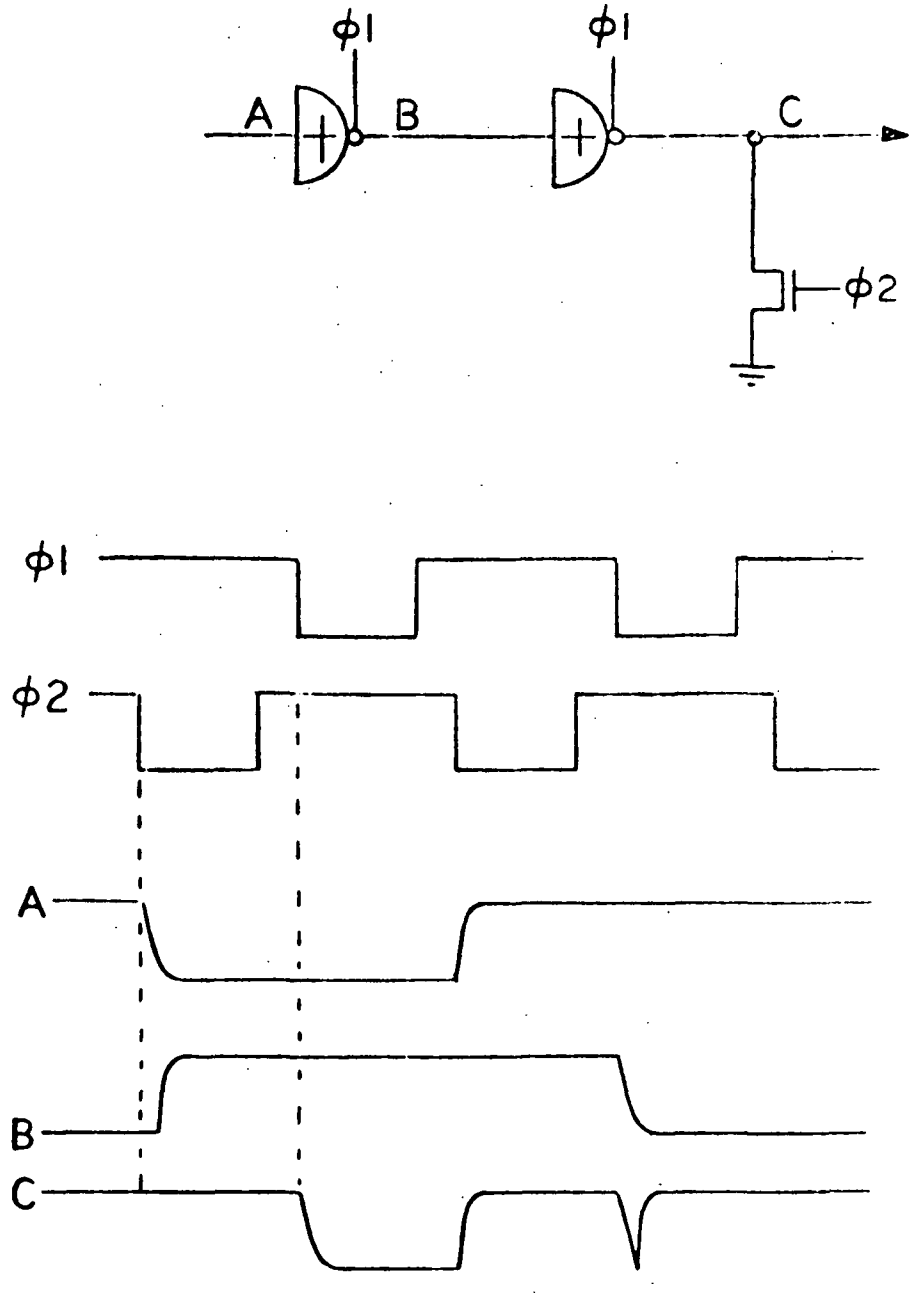


Fig. 10. Sample transient.

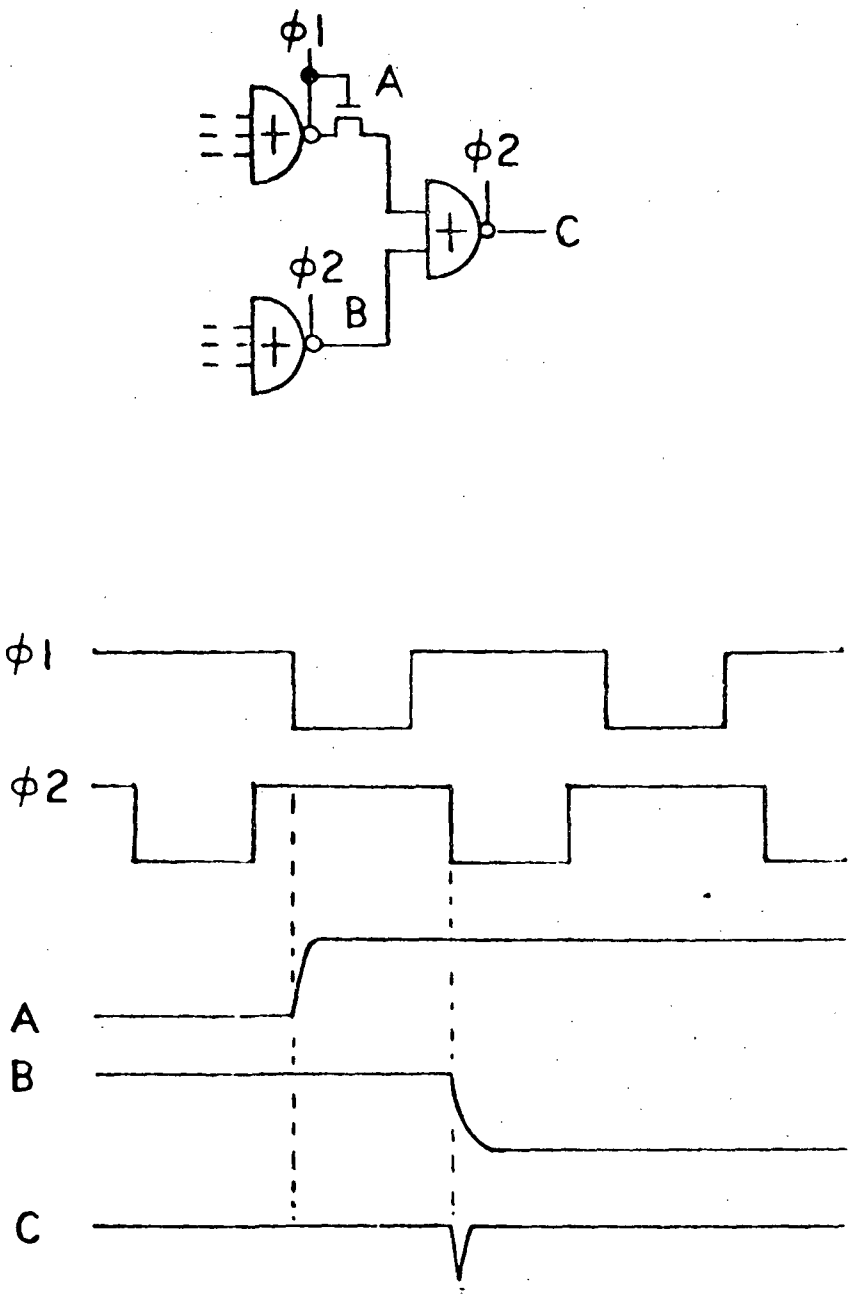


Fig. 11. Internal logic transient.

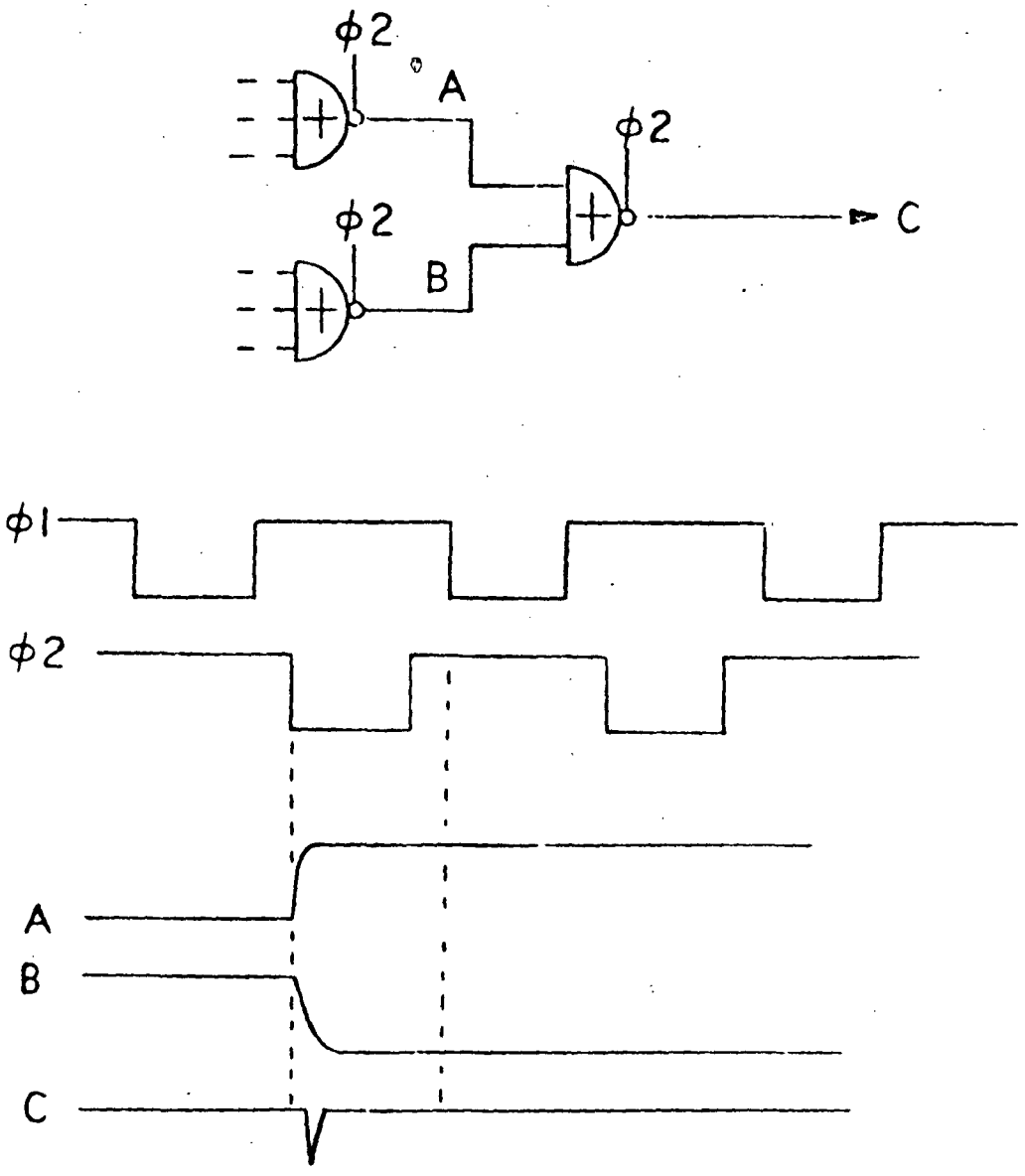


Fig. 12. Internal logic transient.

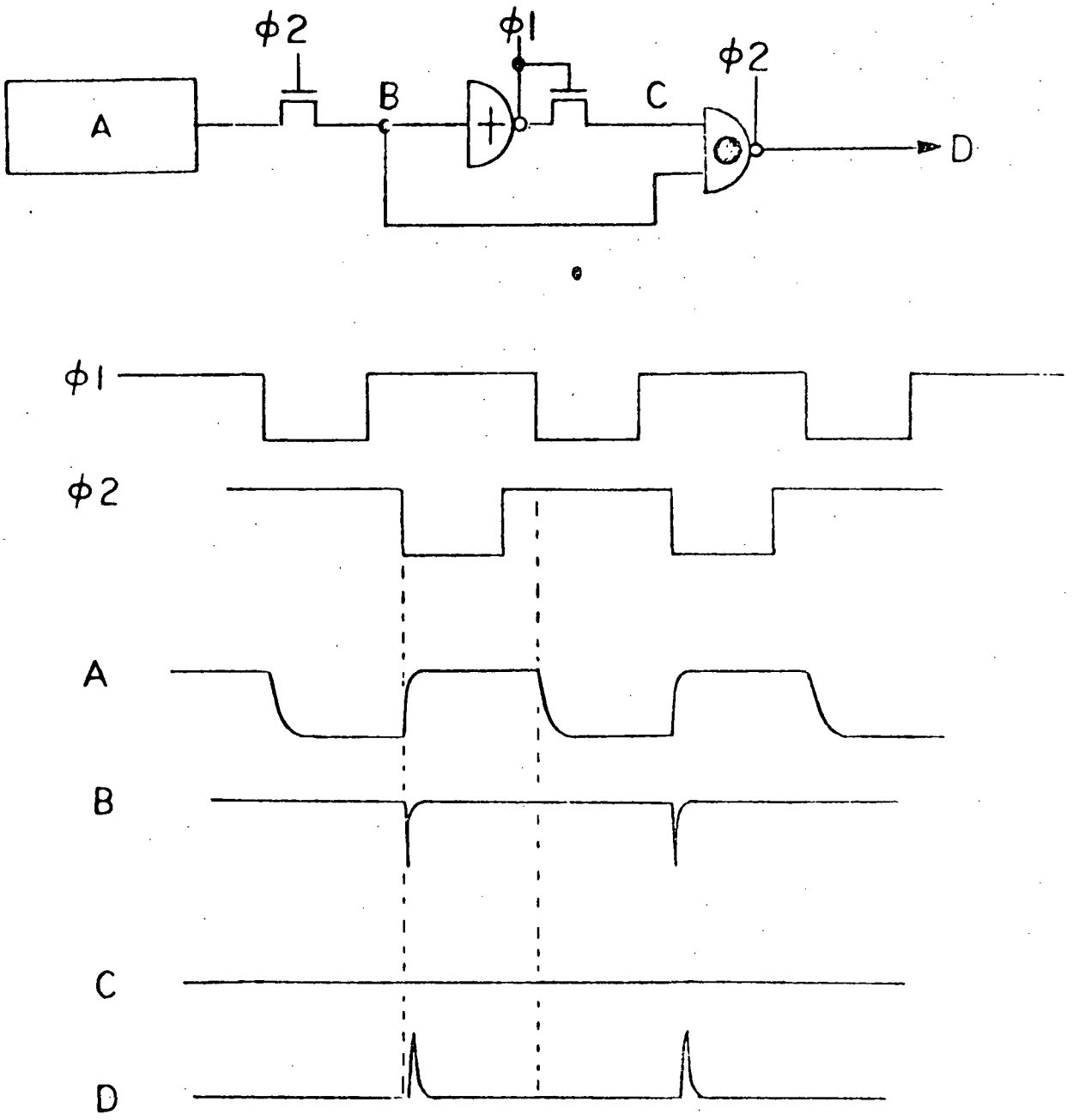


Fig. 13. Differentiation transient.

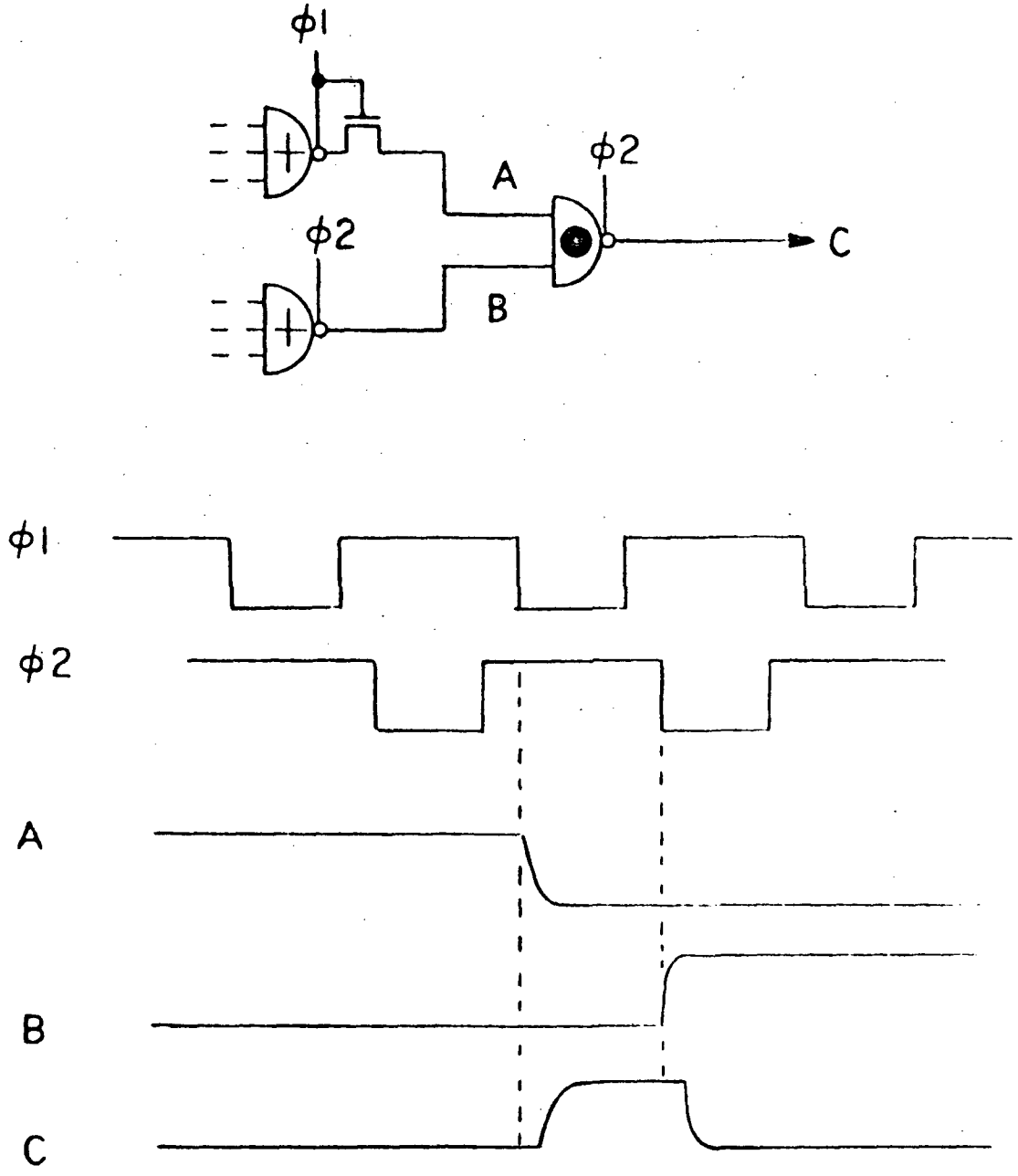


Fig. 14. Internal logic transient.

3.) NAND GATE Without Delay

Here again the output is capable of going to Zero at any clock time depending on the input levels. The output can only go to One on the clock time which operates the load element.

4.) Dynamic Register Stage

These cells provide 1/2-bit-delay to the secondary output and one bit of delay to the primary output, provided the data (or set) inputs change state during the input device clock time ϕ_W. However, if the input or set changes during the output clock time ϕ_X, the secondary output will be delayed one bit time and the primary output will be delayed 1-1/2 bit times from the input change. Due to the many possible input and output conditions, the truth table and logic equations are abbreviated, but both of the above delay conditions are represented.

5.) Static Registers

There are two requirements for a static register which are not shown but are important to its operation. The first is that the shift, or sample pulse, must never be true at the same clock phase as the P output. The reason is simple upon examination. If the sample pulse were One clock period in duration, the leading edge the sample pulse would sample data and the S output would assume its proper state. When the S clock goes off and the P-output clock goes on, the output will always go to Zero due to the sample pulse at the input. On the next clock time, the S output will assume its reset condition. The register will be reset on the last half of the sample pulse each time the sample input occurred. The result is that the sample input must always be grounded during the P-output clock time.

The number of logic levels for each input on a static register is not obvious. The sample input originates on clock phase ϕ_N and propagates through two levels in the static register cell on ϕ_N when referenced to output S. The reset input also propagates through two levels when the input is at ϕ_N and is referenced to output S.

The data input and set input propagate through one level to either output. Figure 15 shows the operation of the static registers.

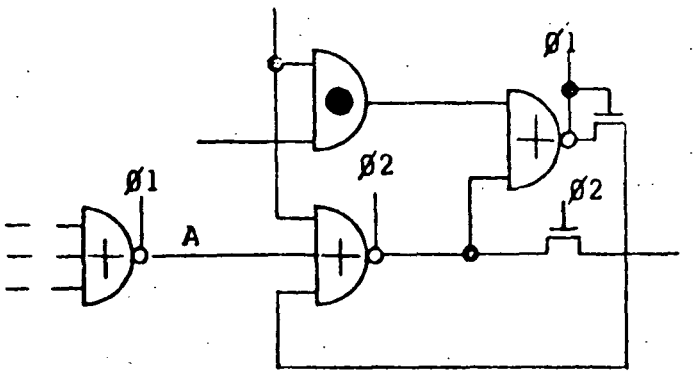


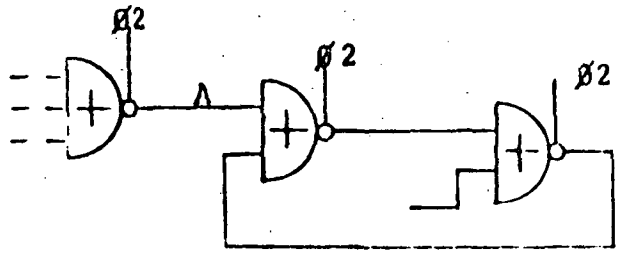
Fig. 15. Static registers. If a 0-1 transient can be produced at A the static register can assume an incorrect or indeterminate state. (solution - eliminate transient or change node A to ϕ2)

6.) Flip-flops

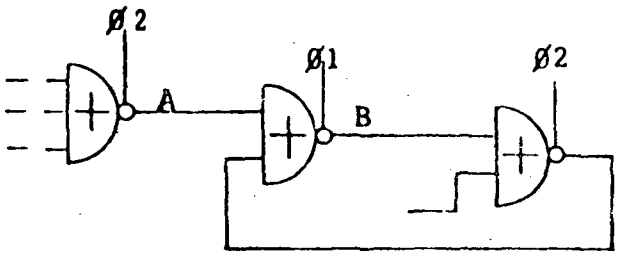
The only requirement on flip-flops that is not shown on the tables is again the possible problem caused by transients on the set and reset lines. In the case of flip-flops both inputs are susceptible to this problem. Figure 16 shows the solution to this problem.

7.) Binary

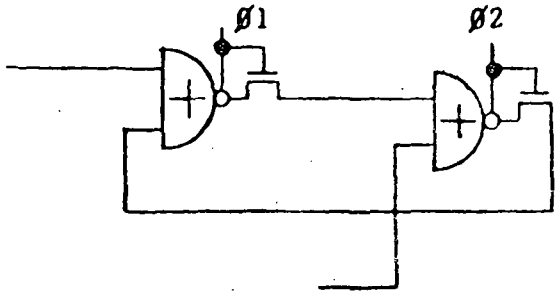
There are two requirements on the binary. If a binary is constructed of other cells to obtain a set input, care must be taken to insure that transients on the set line cannot disrupt the storage of information. The other requirement is on the input line. The binary input controls the binary in three ways. If the input is held to one level, the binary locks up in the state it was in at the time the input went to One. If



(a) If a 0-1 transient can be produced at A, the flip-flop can assume an incorrect or indeterminate state. (solution - eliminate transient)



(b) If a 0-1 transient can be produced at A, the flip-flop can assume an incorrect or indeterminate state. (solution - eliminate transient or add series device at B)



(c) Transient-proof R-S flip-flop.

Fig. 16. R-S flip-flops. If node A comes from an inverter, a 0-1 transient can only occur after node A had been a 1; therefore a double set or reset is produced and no harm is done. Also harmful is a set or reset input from a precharged source.

the input is held at Zero, the binary is made into a single-stage Johnson counter and the clock period is divided by two. In order for the binary to operate as such, however, the input must go to Zero for one clock period only. Each time this occurs the binary will change to the opposite state. Every other time the carry output will go to Zero for one clock period. The carry signal out is the input to the next binary if there is one.

8.) Schmitt

There is but one requirement for the Schmitt trigger. The input must come from a gate whose load device is operated by the clock opposite to that used to feed back around the Schmitt. This is required to allow regeneration in the Schmitt and means that there is always a minimum of 1/2-bit delay through this element.

9.) Precharge Buffer Output

The precharge buffer cell has one input requirement that is important to its proper operation. The input must be such that a 1/2-bit of delay exists in the cell. This means the input transistions must occur at the clock phase opposite to that of the buffer. If this is not done there exists the possibility that the output node may discharge at a time when the node is held to One by the small load device. If this does happen, a faulty output signal will be produced because the small load device will be unable to re-establish the valid One level.

B. DATA SHEETS

The following pages are the data sheets for the BANNING cells. Each cell is depicted by a Data Sheet. The sheets are arranged in ascending order by cell number. Table VII contains a list of all the Cell Numbers together with the corresponding cell widths.

TABLE VII. BANNING CELL WIDTHS AND DRIVING CAPABILITIES

CELL NUMBER	WIDTH (MILS)	ALLOWABLE LOAD (pF) ϕ_i 600 ns. PRIMARY	SECONDARY	TERTIARY
2070-2080	3.6	2.21		
2090-2100	3.6	2.15		
2110-2120	5.0	2.21		
2130-2140	5.0	2.15		
2150-2160	6.4	2.21		
2190-2200	3.6	2.21		
2210-2220	4.2	2.15		
2230-2240	5.0	2.21		
2250-2260	5.0	2.15		
2270-2280	6.4	2.21		
2290-2300	6.4	2.21		
2310-2320	6.4	2.15		
2330-2340	5.0	2.21		
2350-2360	5.0	2.21		
2370-2380	4.6	2.15	2.80	
2390-2400	4.9	2.15		
2410-2420	5.0	2.15		
2440	6.8	2.15		
2460	8.6	2.15	2.80	
2480	10.8	2.15	2.80	
2500	11.3	2.15	2.80	
2520	13.5	2.15	2.80	
2560-2570	7.8	2.15		
2580	4.6	2.15		
2600	6.5	2.15		
2620	6.8	2.15		
2640	10.4	2.15	2.80	
2660	9.9	2.15	2.80	
2680	10.8	2.15	2.80	
2700	12.0	2.15	2.87	2.87
2720	9.9	2.15		
4010-4020	2.2	4.30		
4050-4060	3.0	4.30		
4070-4080	3.6	4.30		
4090-4100	4.1	4.30		
4110-4120	5.0	4.30		
4130-4140	5.7	4.30		
4150-4160	6.4	4.30		
4170-4180	6.8	4.30		
4190-4200	4.5	4.30		
4210-4220	6.6	4.30		
4230-4240	6.2	4.30		
4250-4260	8.6	4.30		
4350-4360	6.0	4.30		

TABLE VII. BANNING CELL WIDTHS AND DRIVING CAPABILITIES (CONTINUED)

CELL NUMBER	WIDTH (MILS)	ALLOWABLE LOAD (pF) ϕ_i 600 ns. PRIMARY	SECONDARY	TERTIARY
4370-4380	6.2	4.30	4.96	
4390-4400	5.2	4.30		
4410-4420	6.2	4.30		
4430	7.8	4.30		
4440	7.1	4.30		
4450	9.4	4.30	2.79	
4460	11.5	4.30	4.96	
4480	13.6	4.30	4.96	
4500	15.7	4.30	4.96	
4520	19.6	4.30	4.96	
4530-4540	6.1	4.30		
4580	4.8	4.30		
4600	6.5	4.30		
4620	7.6	4.30		
4640	14.8	4.30	4.96	
4660	12.5	4.30	4.96	
4680	14.4	4.30	4.96	
5020	1.3	N.A.		
5030-5040	7.5	9.60		
5090	1.8	CAN KILL 20.		
6000-6010	2.2	N.A.		
6020-6030	2.2	N.A.		
6040	1.8	CAN KILL 20.		
6050	2.4	8.00		
6060	7.9	25.00		
6070-6080	5.9	50.00		
6090-6100	8.6	75.00		
6110-6120	10.3	100.00		
6140	6.5	N.A.		
6160	6.4	N.A.		
6180	6.2	.80		
6200	4.3	N.A.		
6220	4.8	N.A.		
6240	5.4	.80		
6250-6260	4.1	11.61		
6270	3.6	N.A.		
6280	3.6	N.A.		
6290-6300	5.4	30.00		
8500	4.8	N.A.		
9034	4.0	N.A.		

All cells are 10.5 mils in height, measured from the bottom of the cell to the center of the V_{LL} bus.

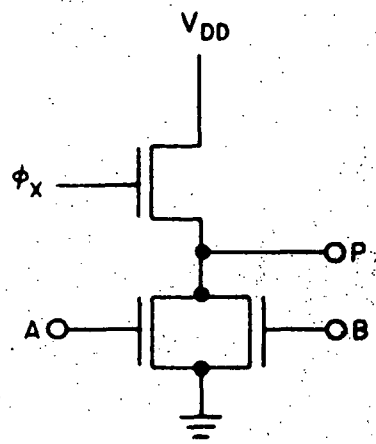
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NOR, 2pF

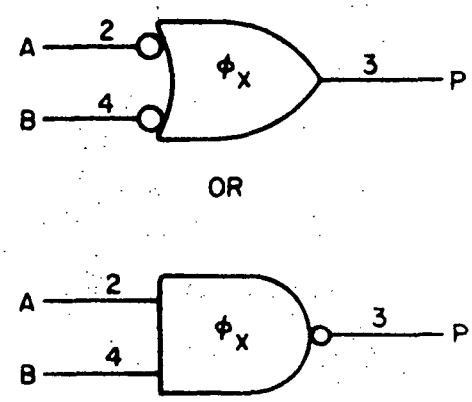
PATTERN NO. 2070 (ϕ_1)
2080 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_X	P
0	0	0	P_{t-1}
1	*	*	0
*	1	*	0
0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

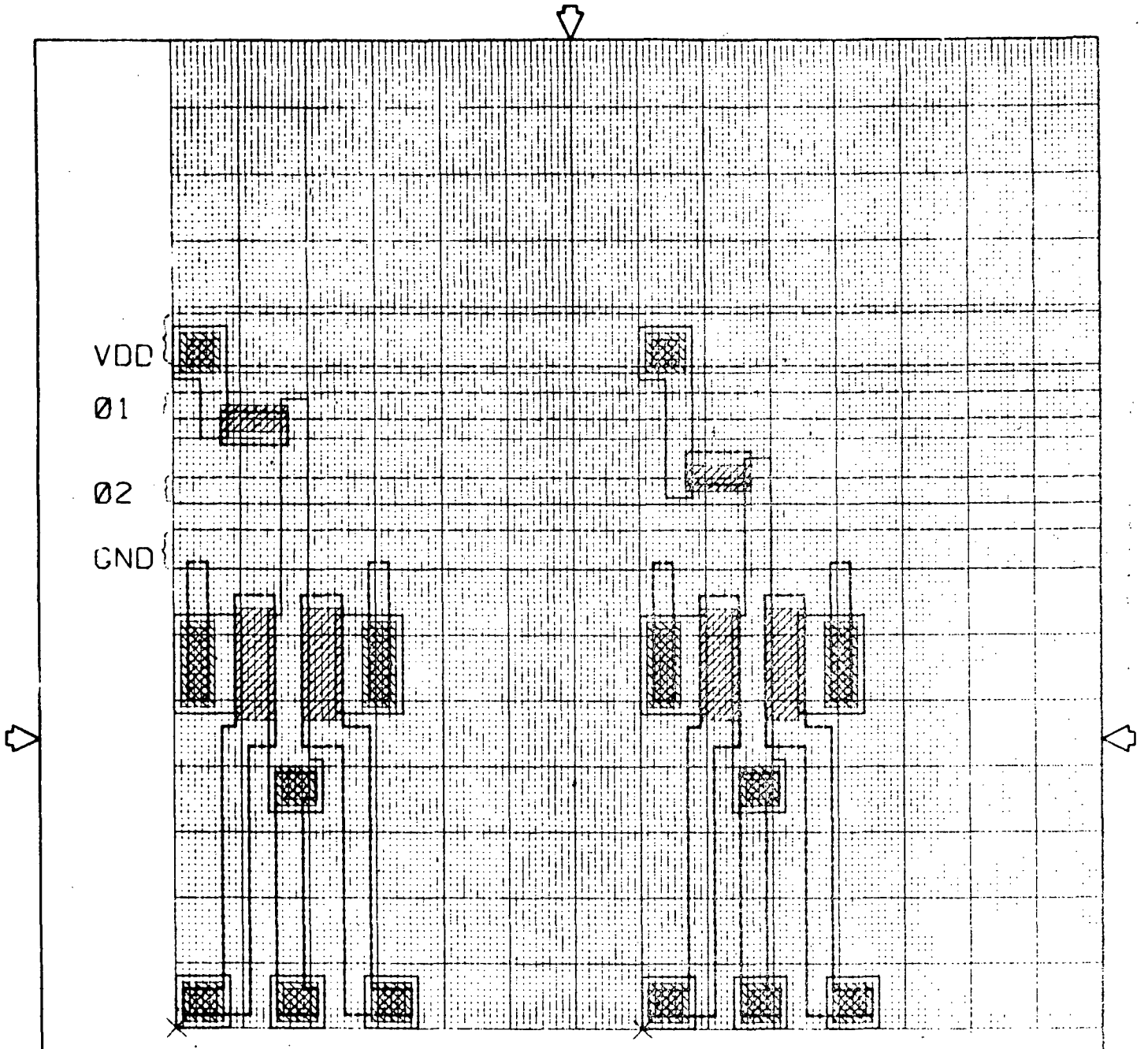
$$P = \overline{(A + B)} \cdot \overline{\phi_X} \cdot P_{t-1} + \overline{(A + B)} \cdot \phi_X$$

$$= \bar{A} \cdot \bar{B} \cdot \overline{\phi_X} \cdot P_{t-1} + \bar{A} \cdot \bar{B} \cdot \phi_X$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	290	290
C_P	3	300	270
C_B	4	290	290
PATTERN NO.		2070	2080

TWO INPUT NOR • 2070 2080 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		2 INPUT NOR
SCALE 0.1mil/div			SHEET

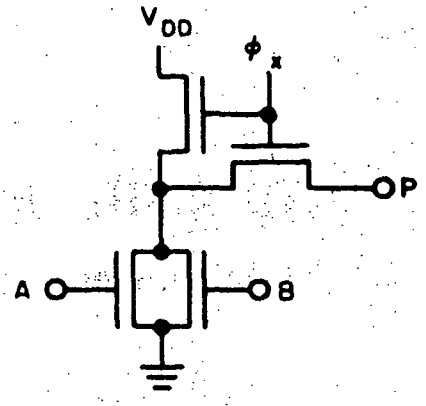
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NOR WITH DELAY, 2pF

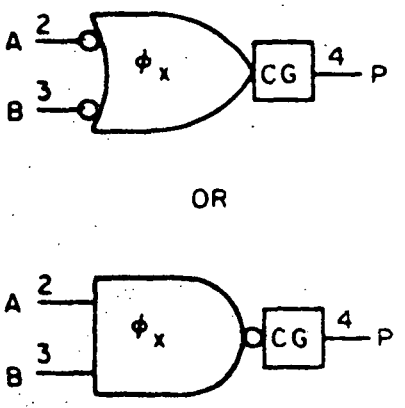
PATTERN NO. 2090 (ϕ_1)
2100 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
*	*	0	P_{t-1}
1	*	1	0
*	1	1	0
0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi_x} + \overline{(A + B)} \cdot \phi_x$$

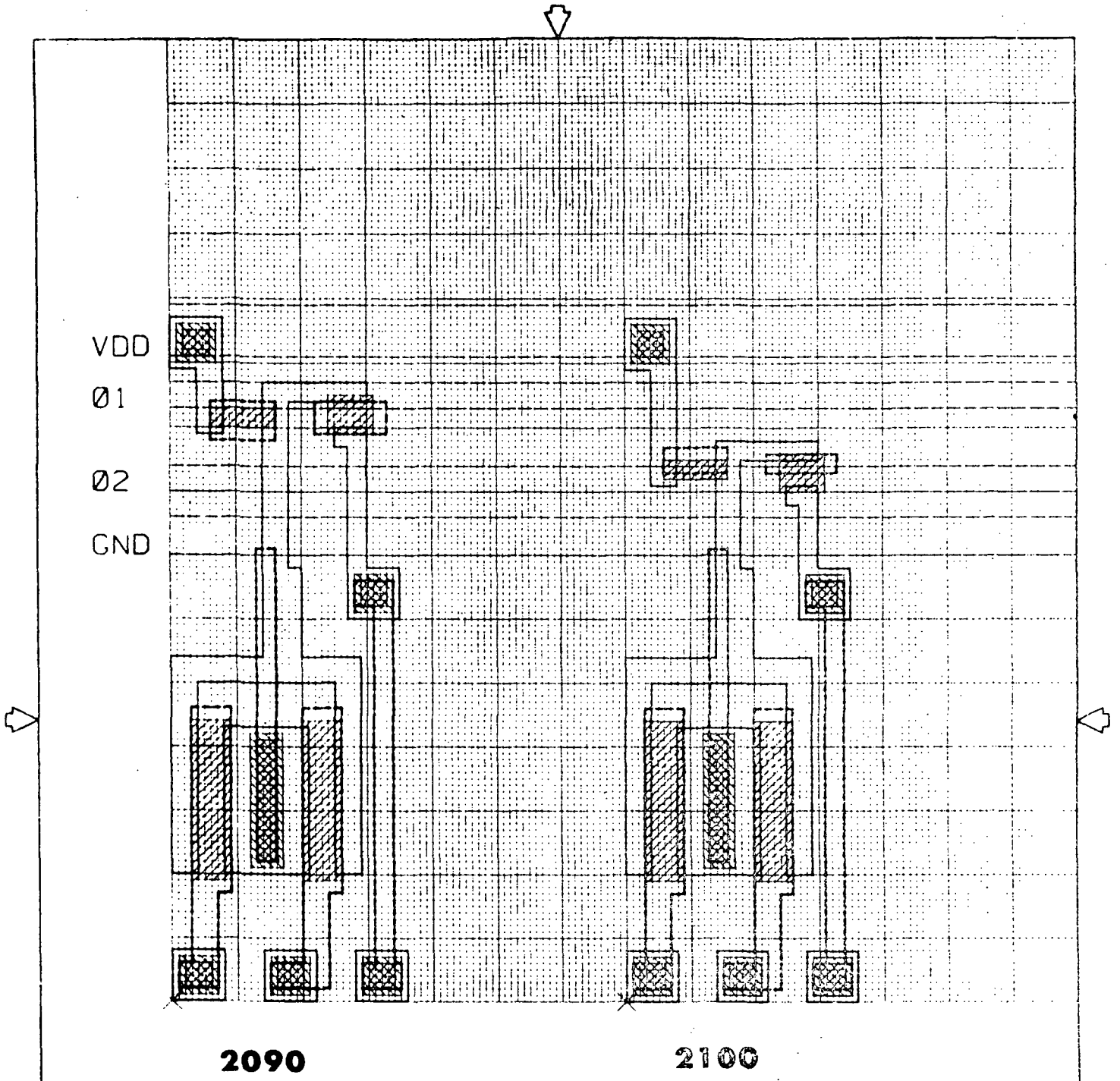
$$= (P_{t-1}) \cdot \overline{\phi_x} + \overline{A} \cdot \overline{B} \cdot \phi_x$$

PATTERN NO.

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	360	360
C_B	3	360	360
C_P	4	480	450
PATTERN NO.		2090	2100

TWO INPUT NOR WITH DELAY • 2090 2100 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NOR W/DLY
SCALE 0.1 mil/div		SHEET

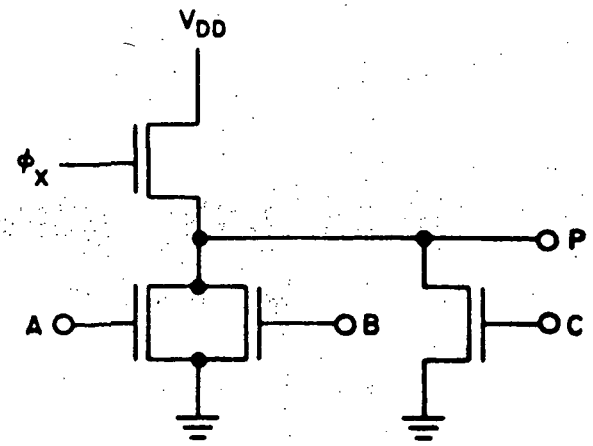
BANNING THICK OXIDE STANDARD CELL

THREE INPUT NOR, 2pF

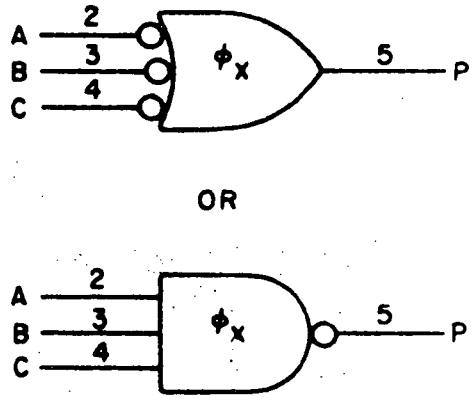
PATTERN NO. 2110 (ϕ_1)
2120 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
0	0	0	0	P_{t-1}
1	*	*	*	0
*	1	*	*	0
*	*	1	*	0
0	0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

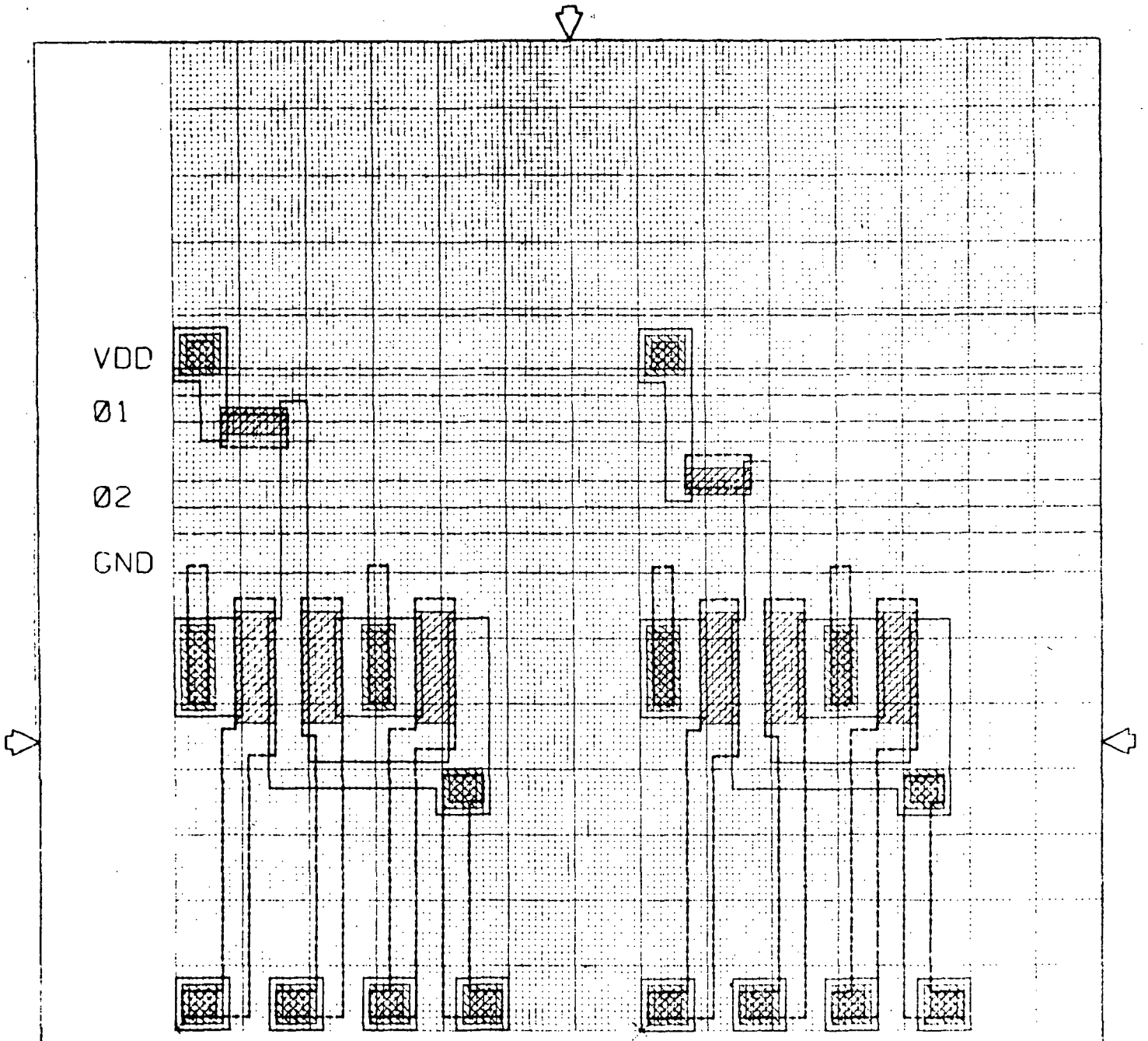
$$P = (P_{t-1}) \cdot \bar{\phi}_x \cdot \overline{(A + B + C)} + \overline{(A + B + C)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{\phi}_x \cdot \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	290	290
C_B	3	290	290
C_C	4	290	290
C_P	5	460	440
PATTERN NO.		2110	2120

THREE INPUT NOR • 2110 2120 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT NOR
SCALE 0.1 mil/div		SHEET

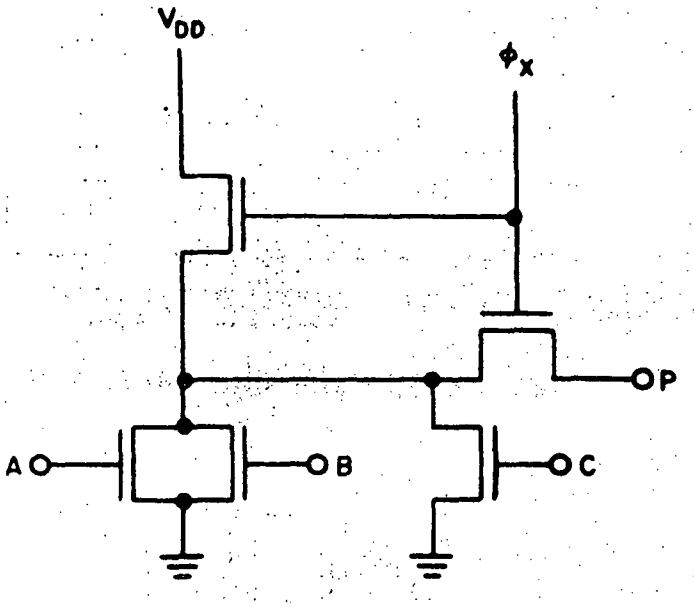
BANNING THICK OXIDE STANDARD CELL

THREE INPUT NOR WITH DELAY, .2pF

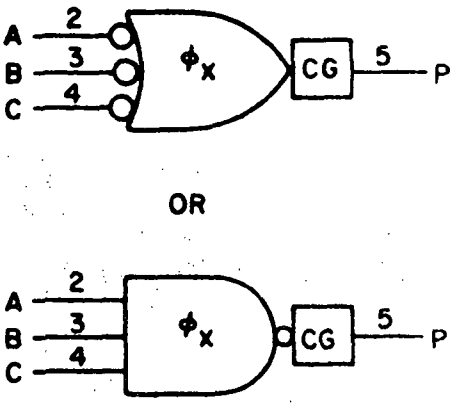
PATTERN NO. 2130 (ϕ_1)
2140 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
*	*	*	0	P_{t-1}
1	*	*	1	0
*	1	*	1	0
*	*	1	1	0
0	0	0	1	1

*MEANS EITHER STATE

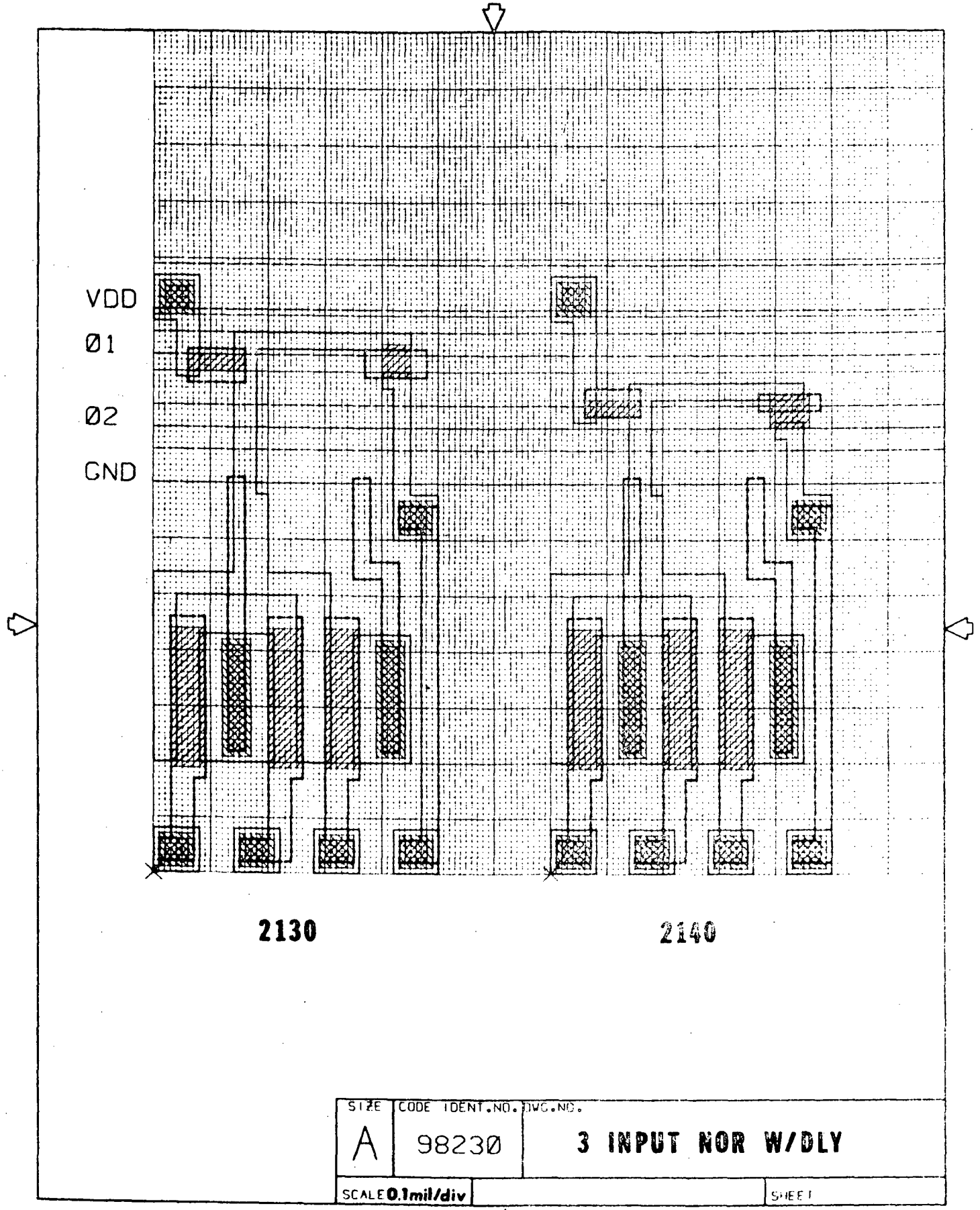
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{\phi}_x + \overline{(A + B + C)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{\phi}_x + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	360	360
C_B	3	360	360
C_C	4	350	360
C_P	5	550	510
PATTERN NO.		2130	2140



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT NOR W/DLY
SCALE 0.1mil/div		SHEET

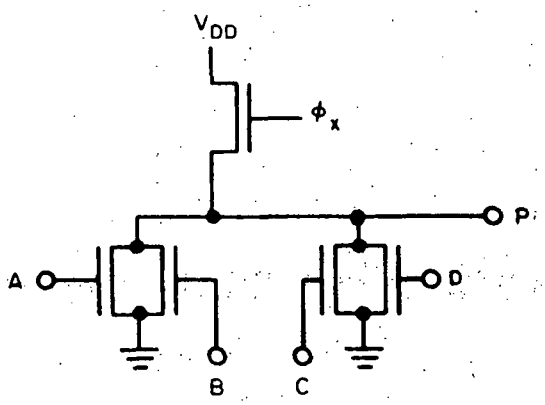
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT NOR, 2pF

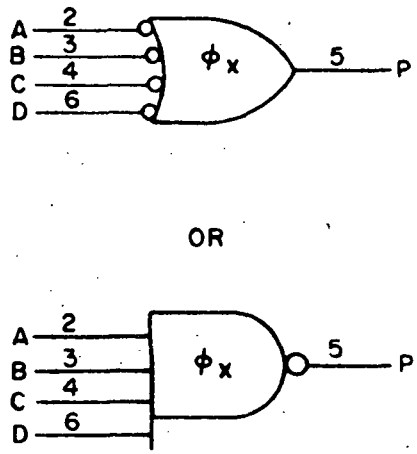
PATTERN NO. 2150 (ϕ_1)
2160 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	ϕ_x	P
0	0	0	0	0	P_{t-1}
1	*	*	*	*	0
*	1	*	*	*	0
*	*	1	*	*	0
*	*	*	1	*	0
0	0	0	0	1	1

*MEANS EITHER STATE

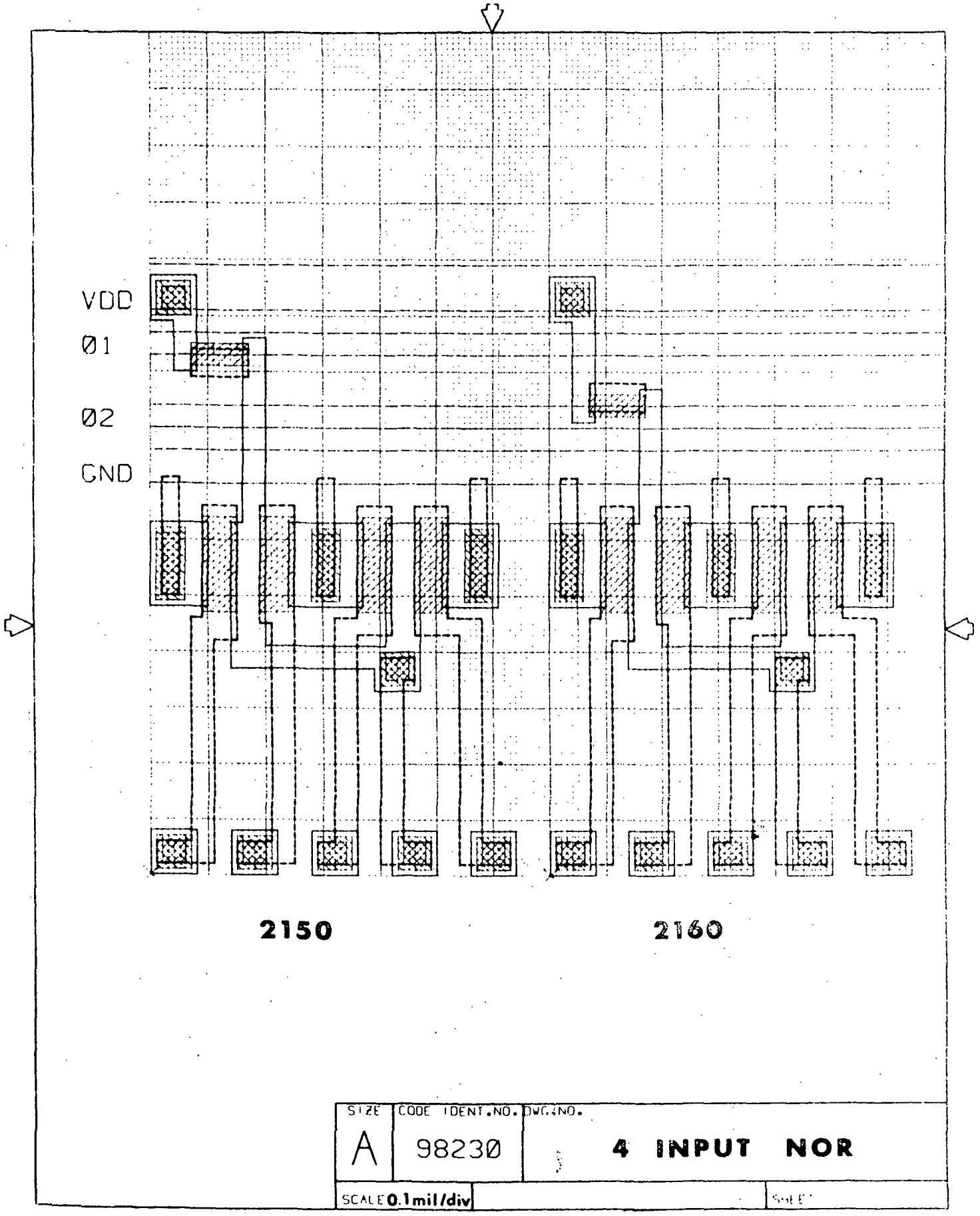
LOGIC EQUATIONS

$$P = P_{t-1} \cdot (\overline{A + B + C + D}) \cdot \overline{\phi_x} + (\overline{A + B + C + D}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \overline{\phi_x} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	290	290
C_B	3	290	290
C_C	4	290	290
C_P	5	460	440
C_D	6	290	290
PATTERN NO.		2150	2160



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		4 INPUT NOR
SCALE 0.1 mil/div			SHEET

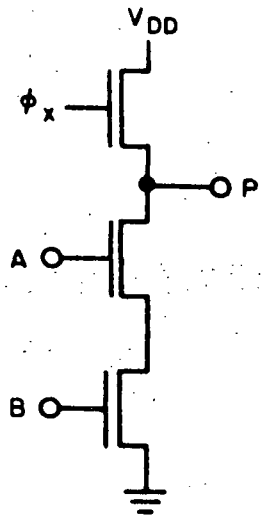
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NAND, 2pF

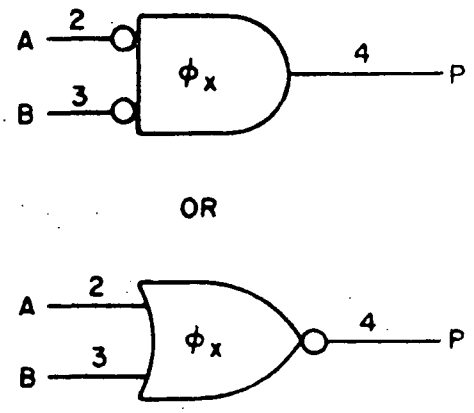
PATTERN NO. 2190 (ϕ_1)
2200 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
0	*	0	P_{t-1}
*	0	0	P_{t-1}
1	1	*	0
0	*	1	1
*	0	1	1

*MEANS EITHER STATE

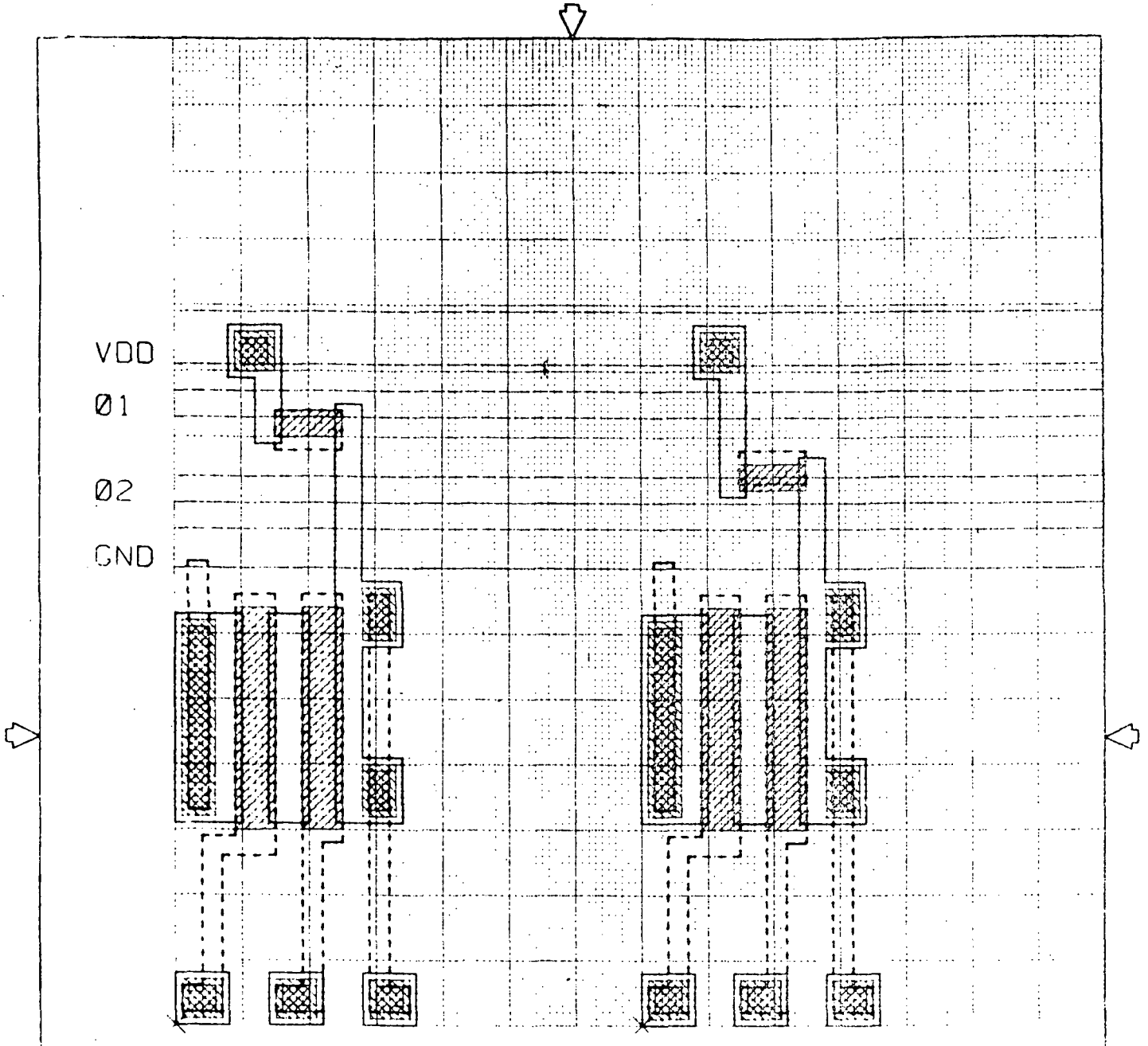
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot (\overline{A \cdot B}) \cdot \overline{\phi}_x + (\overline{A \cdot B}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\bar{A} + \bar{B}) \cdot \overline{\phi}_x + (\bar{A} + \bar{B}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	620	630
C_B	3	630	620
C_P	4	510	460
PATTERN NO.		2190	2200



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NAND 2PF
SCALE 0.1mil/div		SHEET

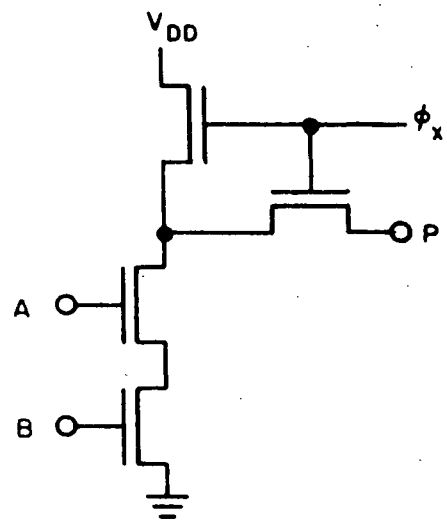
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NAND WITH DELAY, 2pF

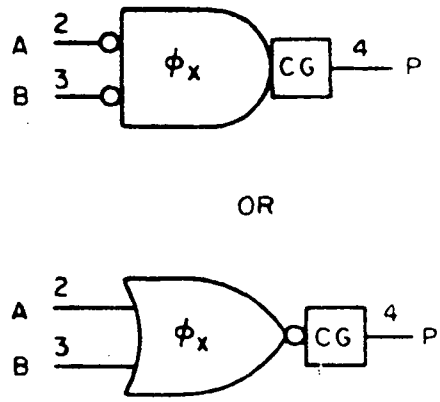
PATTERN NO. 2210 (ϕ_1)
2220 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
*	*	0	P_{t-1}
1	1	1	0
0	*	1	1
*	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

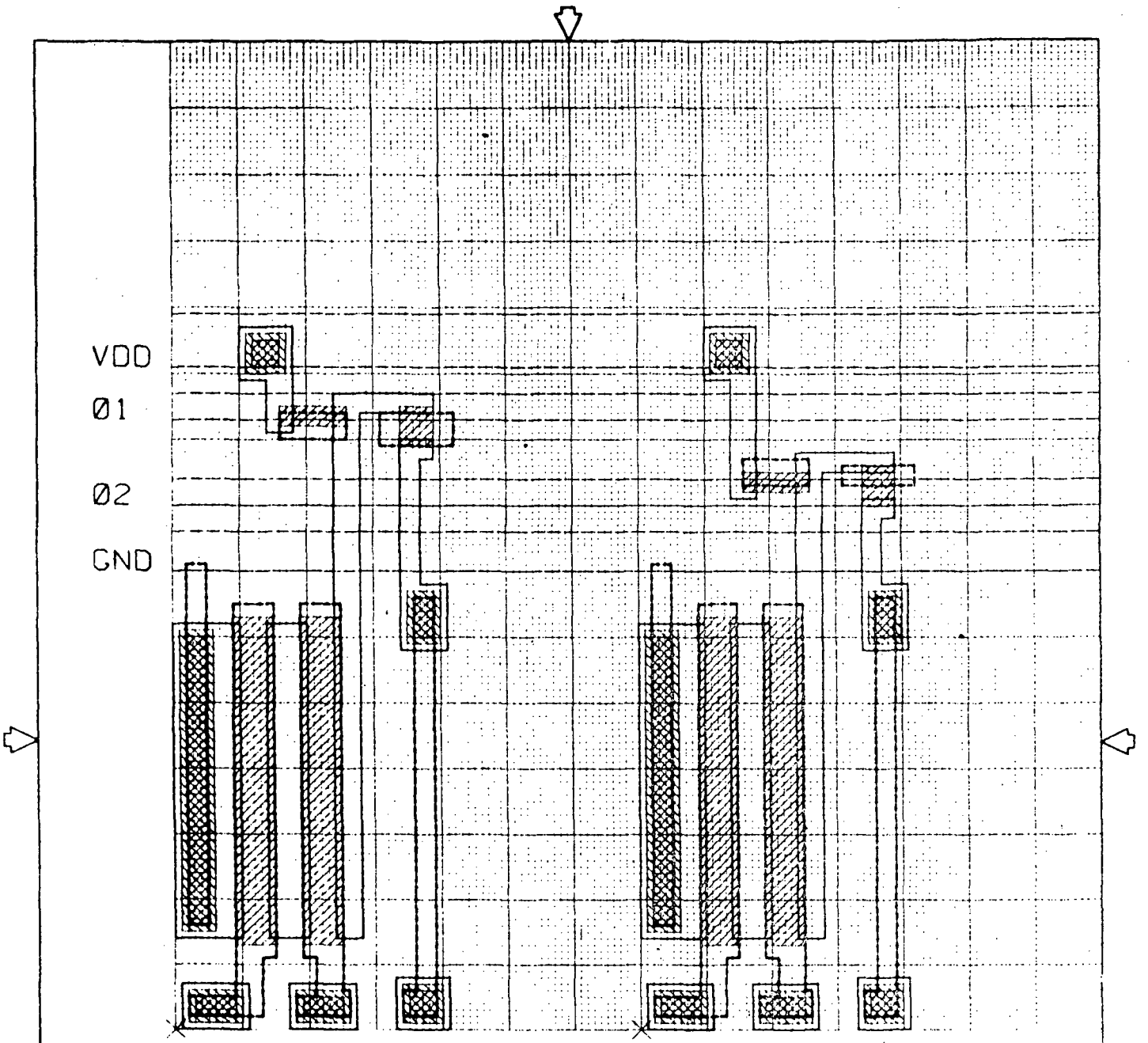
$$P = (P_{t-1}) \cdot \bar{\phi}_x + (\overline{A \cdot B}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{\phi}_x + (\bar{A} + \bar{B}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	660	660
C_B	3	660	660
C_P	4	180	160
PATTERN NO.		2210	2220

TWO INPUT NAND WITH DELAY • 2210 2220 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NAND W/DLY
SCALE 0.1mil/div		SHEET

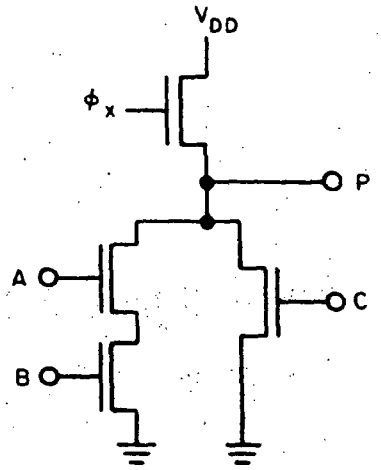
BANNING THICK OXIDE STANDARD CELL

THREE INPUT AND NOR, 2pF

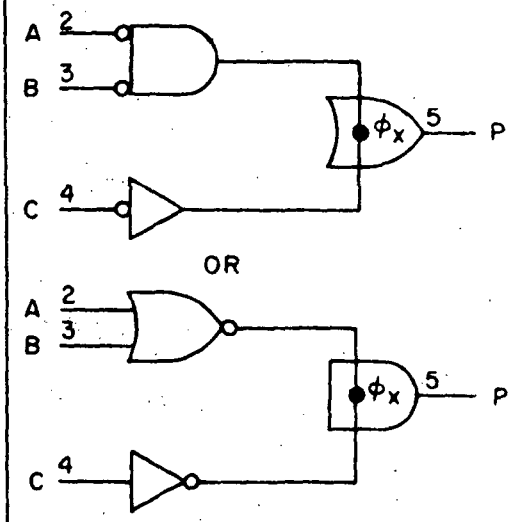
PATTERN NO. 2230 [ϕ_1]
2240 [ϕ_2]

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
0	*	0	0	P_{t-1}
*	0	0	0	P_{t-1}
*	*	1	*	0
1	1	*	*	0
0	*	0	1	1
*	0	0	1	1

*MEANS EITHER STATE

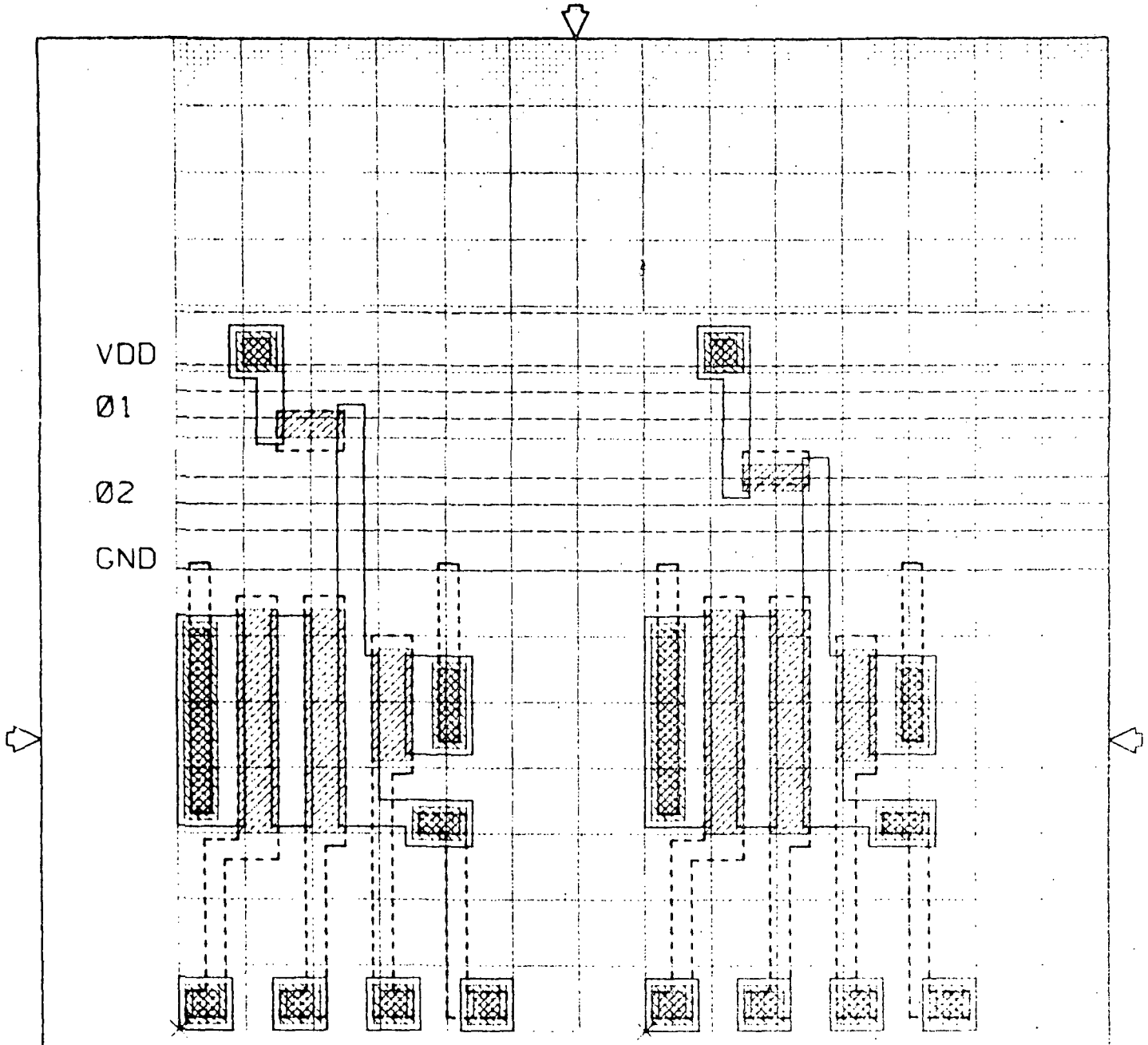
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot (\overline{A \cdot B + C}) \cdot \overline{\phi_x} + (\overline{A \cdot B + C}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \overline{\phi_x} + (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	630	630
C_B	3	620	620
C_C	4	390	390
C_P	5	560	510
PATTERN NO.		2230	2240



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3INPUT AND NOR 2PF
SCALE 0.1mil/div		SHEET

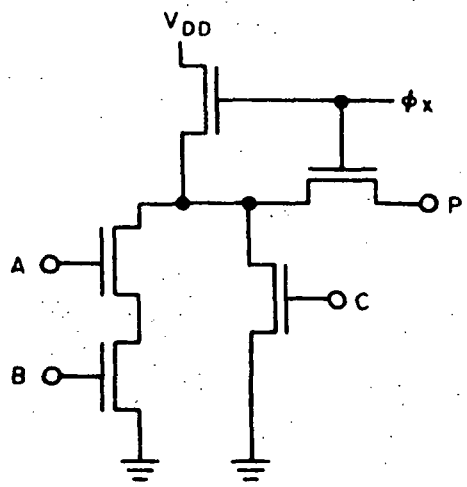
BANNING THICK OXIDE STANDARD CELL

THREE INPUT AND NOR WITH DELAY, 2pF

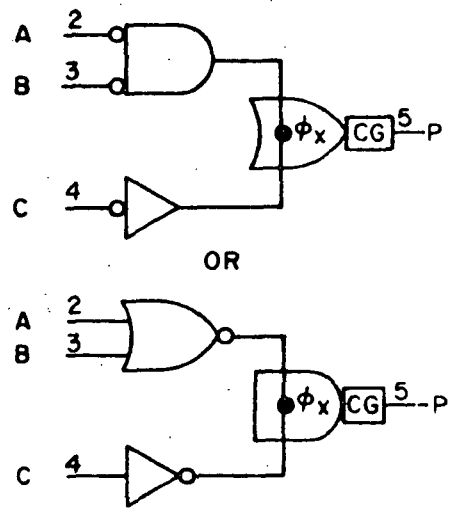
PATTERN NO. 2250 [ϕ_1]
2260 [ϕ_2]

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
*	*	*	0	P_{t-1}
*	*	1	1	0
1	1	*	1	0
0	*	0	1	1
*	0	0	1	1

*MEANS EITHER STATE

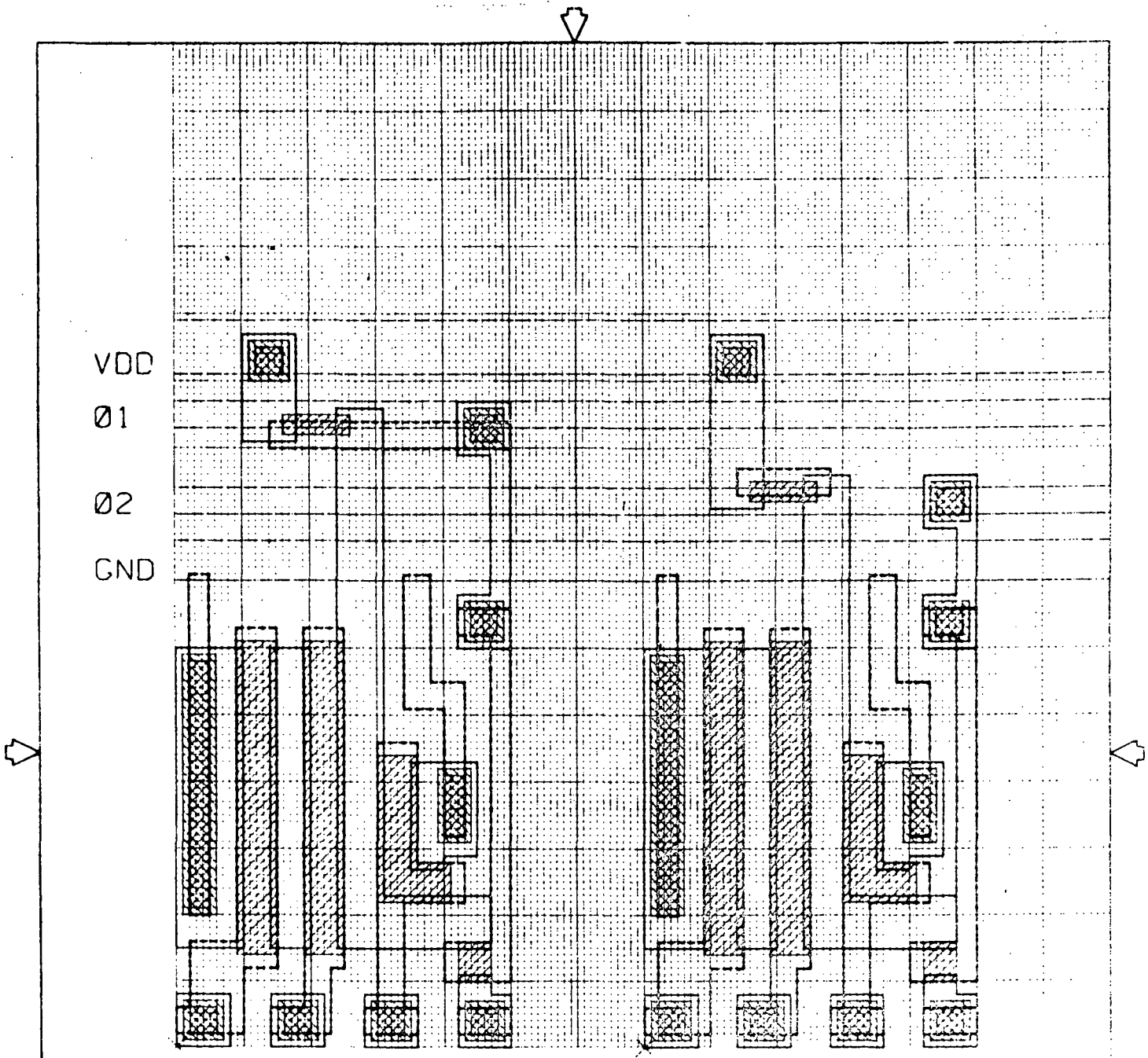
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{\phi}_x + (\overline{A \cdot B + C}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{\phi}_x + (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	630	630
C_B	3	620	620
C_C	4	380	380
C_P	5	420	380
PATTERN NO.		2250	2260



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT AND NOR W/DLY
SCALE 0.1 mil/div		SHEET

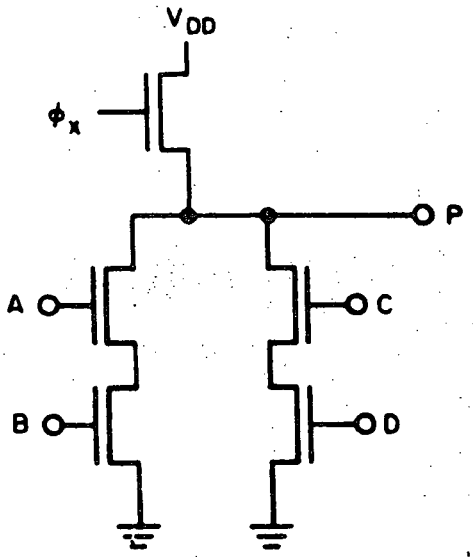
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT NAND OR, 2pF

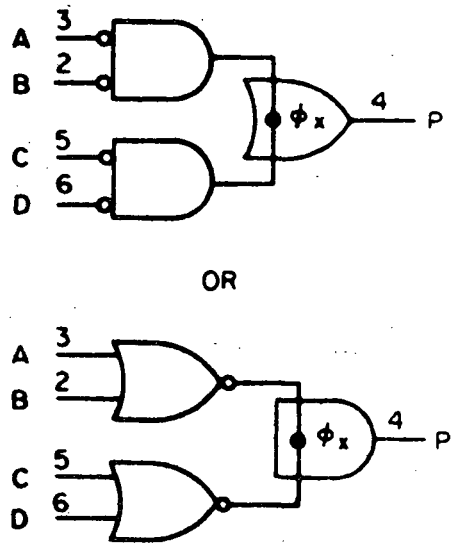
PATTERN NO. 2270 (ϕ_1)
2280 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A · B	C · D	ϕ_x	P
0	0	0	P_{t-1}
*	1	*	0
1	*	*	0
0	0	1	1

*MEANS EITHER STATE

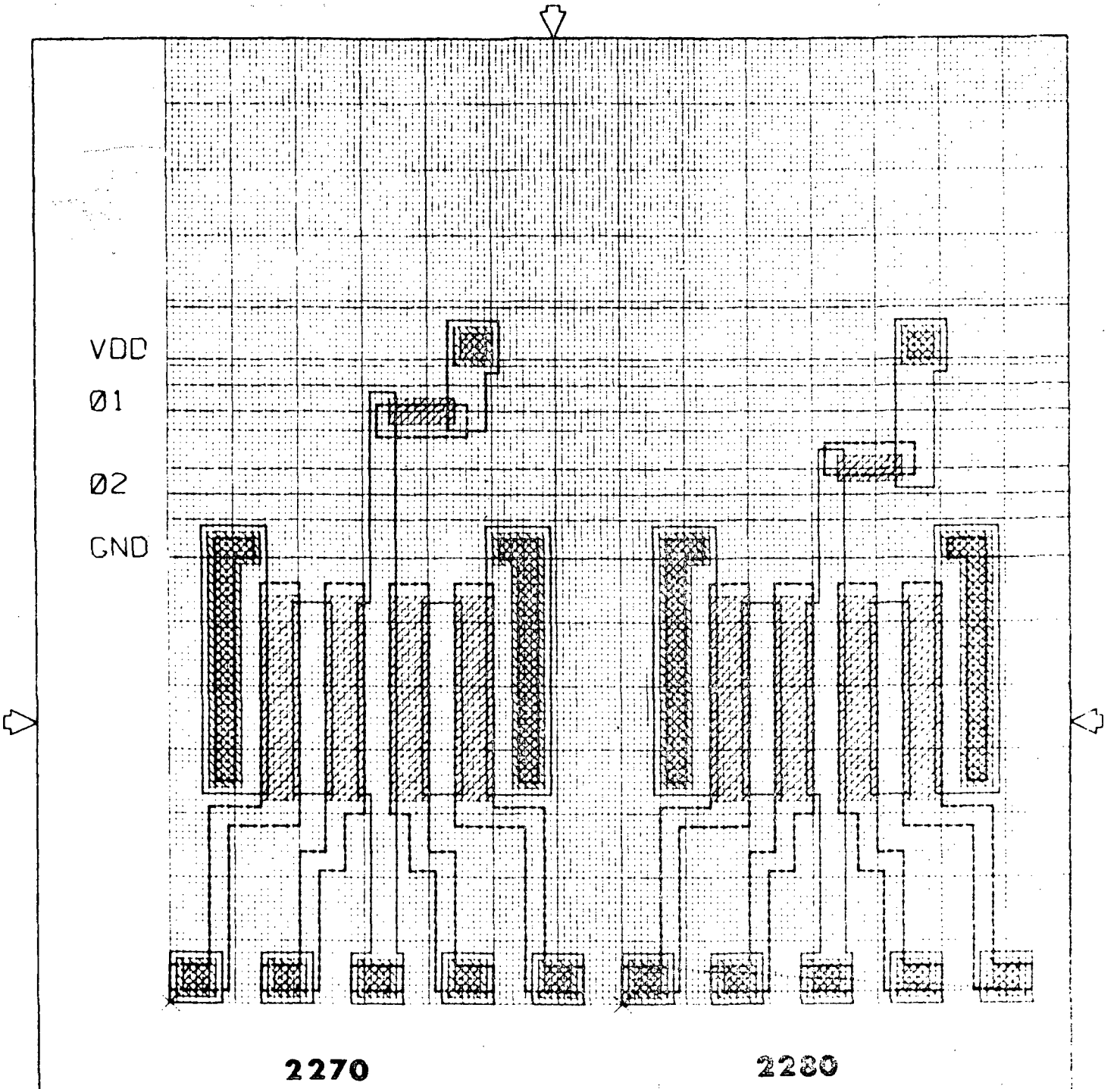
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{(A \cdot B + C \cdot D)} \cdot \bar{\phi}_x + \overline{(A \cdot B + C \cdot D)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D}) \cdot \bar{\phi}_x + (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_B	2	450	450
C_A	3	460	460
C_P	4	330	310
C_C	5	450	450
C_D	6	460	460
PATTERN NO.		2270	2280



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	4 INPUT NAND OR
SCALE 0.1 mil/div		SHEET

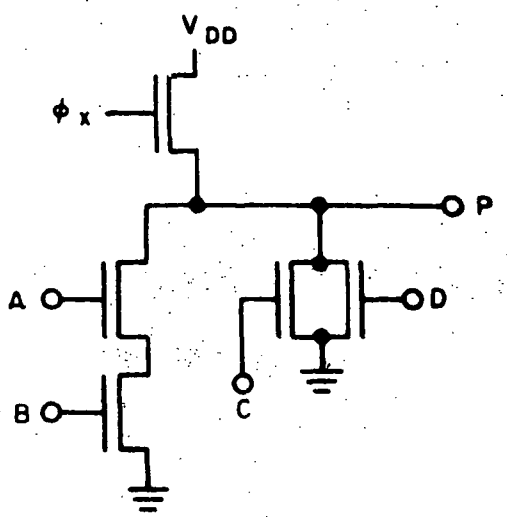
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT AND NOR, 2pF

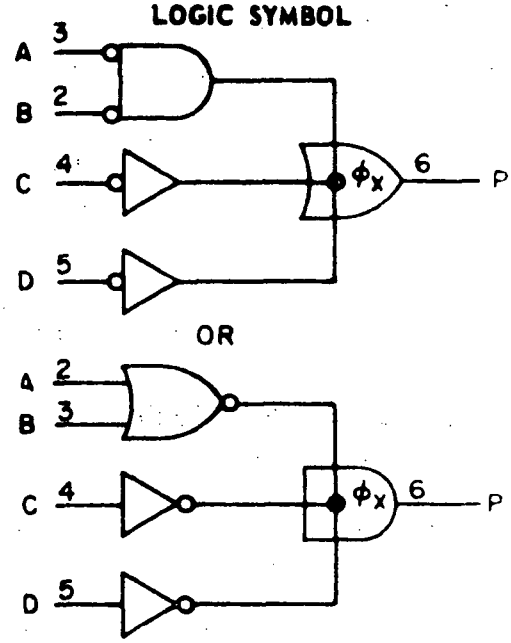
PATTERN NO. 2290 (ϕ_1)
2300 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A · B	C	D	ϕ_x	P
0	0	0	0	P_{t-1}
*	*	1	*	0
*	1	*	*	0
1	*	*	*	0
0	0	0	1	1

*MEANS EITHER STATE

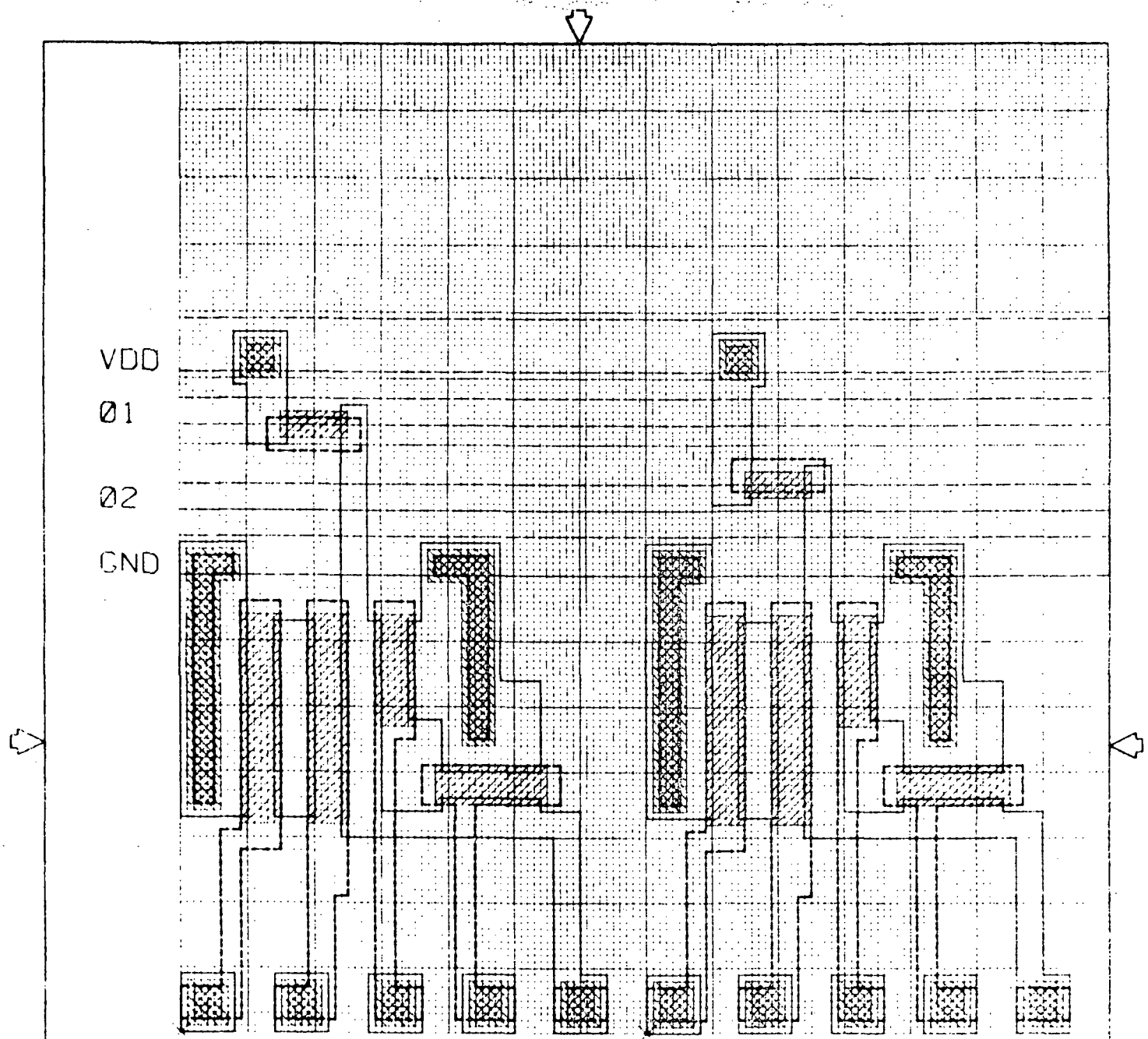
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{(A \cdot B + C + D)} \cdot \overline{\phi_x} + \overline{(A \cdot B + C + D)} \cdot \phi_x$$

$$= (P_{t-1}) \, \overline{(A \cdot B)} \cdot \bar{C} \cdot \bar{D} \cdot \overline{\phi_x} + \overline{(A \cdot B)} \cdot \bar{C} \cdot \bar{D} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_B	2	460	460
C_A	3	460	450
C_C	4	280	280
C_D	5	280	270
C_P	6	450	420
PATTERN NO.		2290	2300



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	**4 INPUT AND NOR**	
SCALE **0.1 mil/div**			SHEET

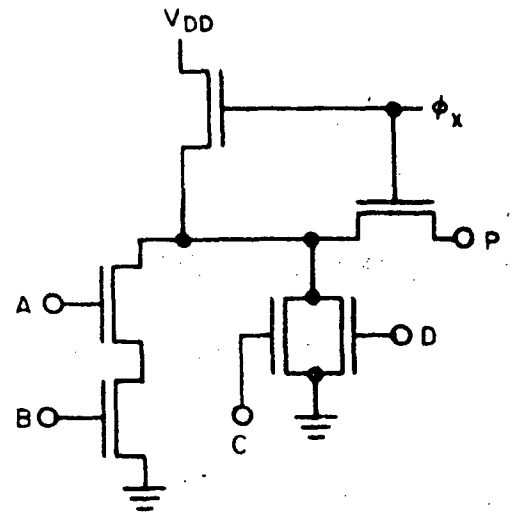
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT AND NOR WITH DELAY, 2pF

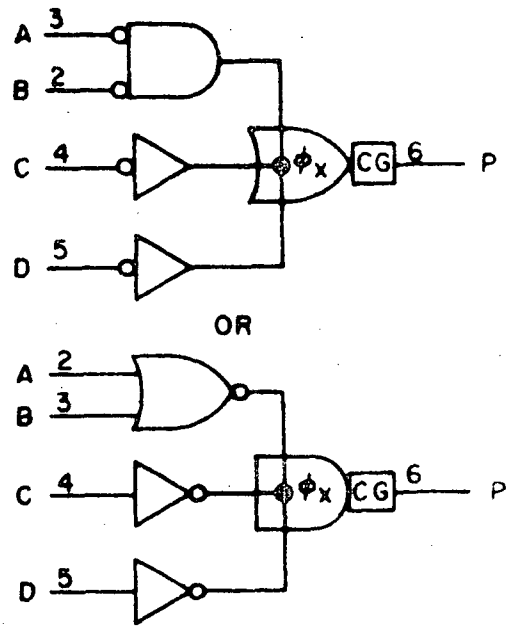
PATTERN NO. 2310 (ϕ_1)
2320 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A · B	C	D	ϕ_x	P
*	*	*	0	P_{t-1}
*	*	1	1	0
*	1	*	1	0
1	*	*	1	0
0	0	0	1	1

*MEANS EITHER STATE

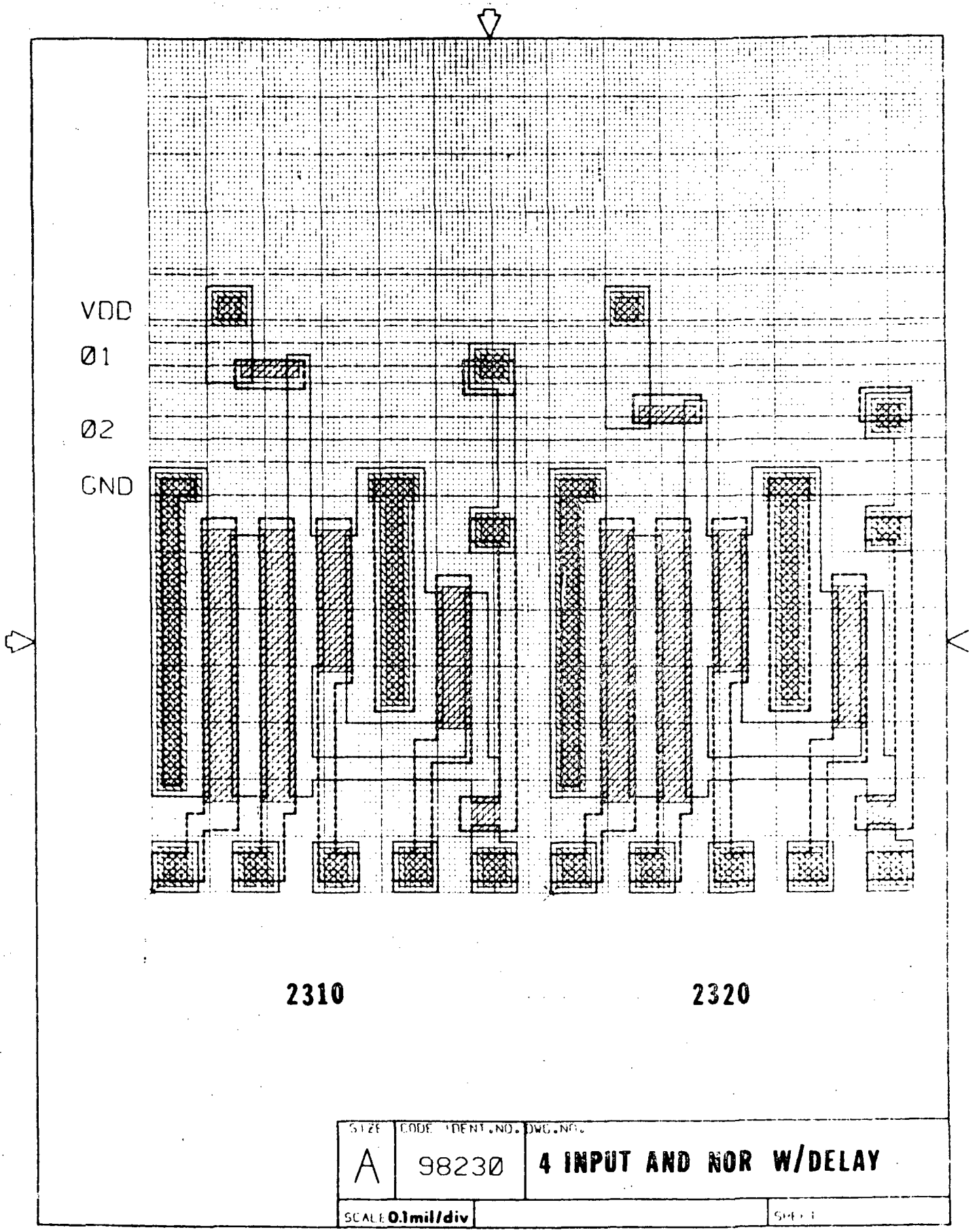
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi}_x + \overline{(A \cdot B + C + D)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot \overline{\phi}_x + (\overline{A \cdot B}) \cdot \overline{C} \cdot \overline{D} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_B	2	640	640
C_A	3	640	640
C_C	4	380	370
C_D	5	370	370
C_P	6	390	370
PATTERN NO.		2310	2320



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	4 INPUT AND NOR W/DELAY	
SCALE 0.1mil/div			SHEET

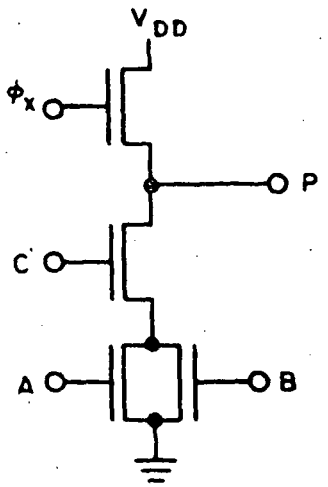
BANNING THICK OXIDE STANDARD CELL

THREE INPUT OR NAND, 2pF

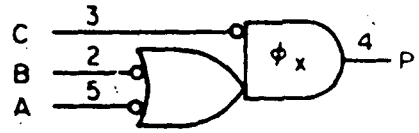
PATTERN NO. 2330 (ϕ_1)
2340 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

C	A	B	ϕ_x	P
0	*	*	0	P_{t-1}
1	0	0	0	P_{t-1}
1	1	*	*	0
1	*	1	*	0
0	*	*	1	1
*	0	0	1	1

*MEANS EITHER STATE

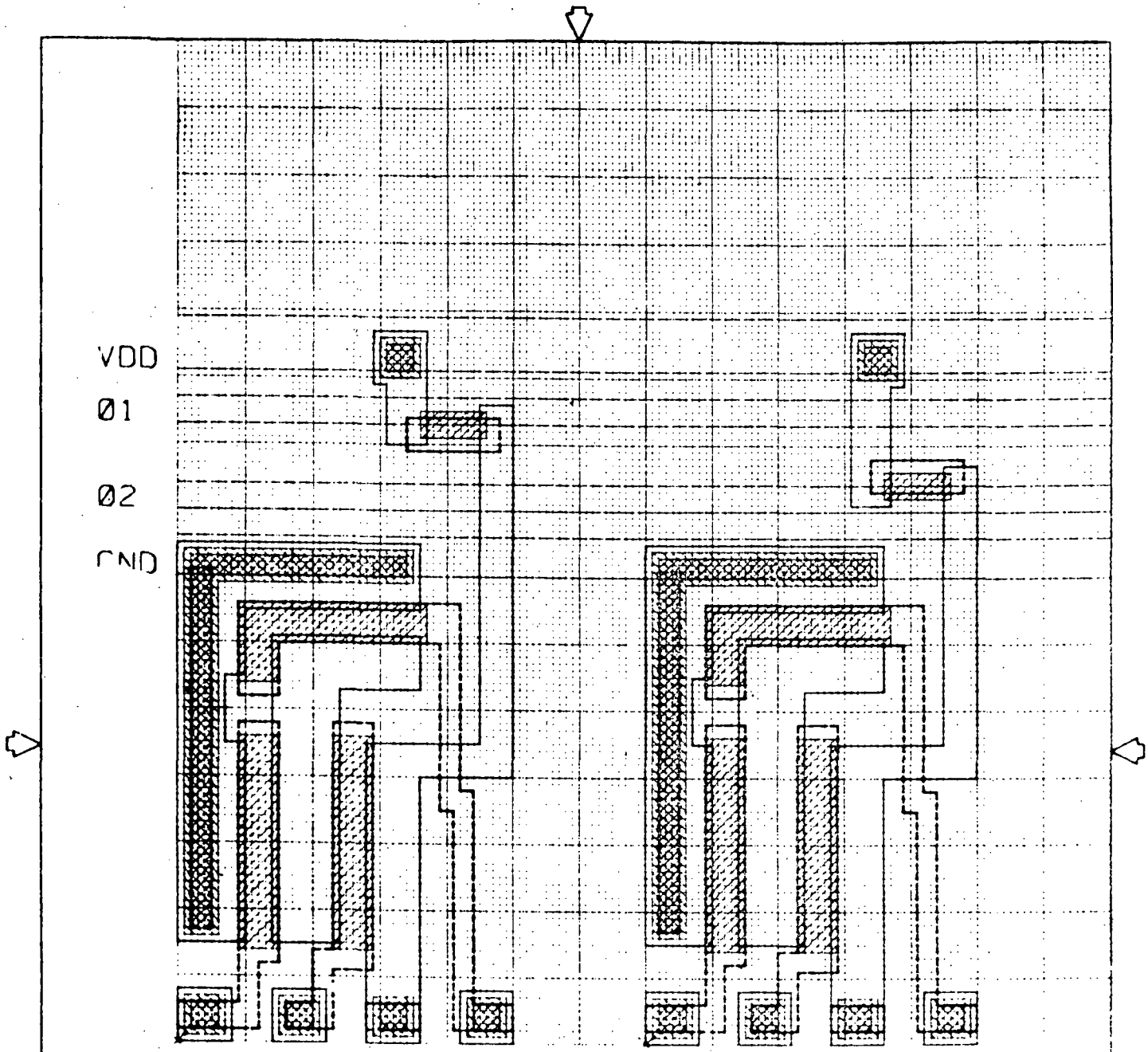
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{(C \cdot [A + B])} \cdot \overline{\phi}_x + \overline{C \cdot (A + B)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\bar{C} + \bar{A}\,\bar{B}) \cdot \overline{\phi}_x + (\bar{C} + \bar{A}\bar{B}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_B	2	440	440
C_C	3	440	440
C_P	4	480	450
C_A	5	500	500
PATTERN NO.		2330	2340



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT OR NAND
SCALE 0.1mil/div		SHEET

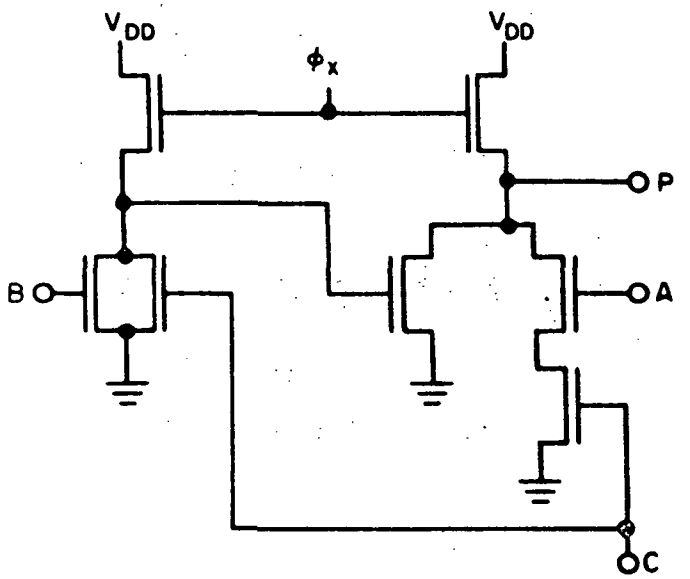
BANNING THICK OXIDE STANDARD CELL

THREE INPUT SWITCH, 2pF
(OPTIONAL EXCLUSIVE OR)

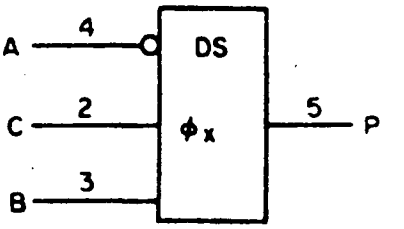
PATTERN NO. 2350 (ϕ_1)
2360 (ϕ_2)

APRIL 1968

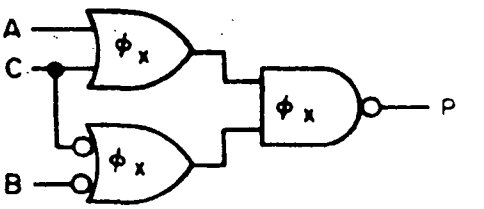
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	C	ϕ_x	P
·	·	0	0	P_{t-1}
0	·	·	0	P_{t-1}
1	·	1	·	0
·	0	0	1	0
·	1	0	1	1
0	·	1	1	1

·MEANS EITHER STATE

LOGIC EQUATIONS

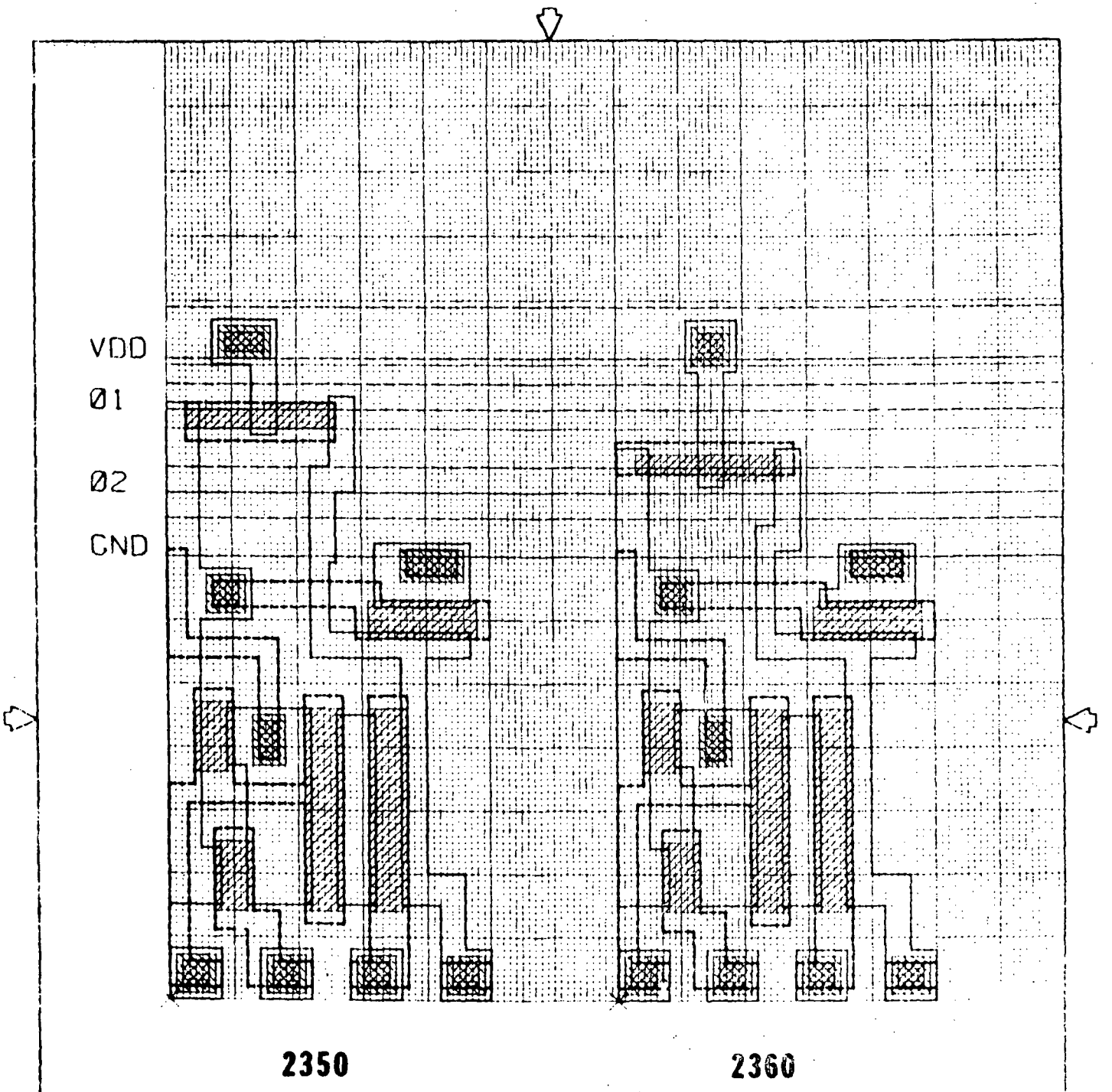
$$P = (P_{t-1}) \cdot (\bar{A} + \bar{C}) \cdot \bar{\phi}_x \, (B\bar{C} + \bar{A}\,[B + C])$$

FOR EXCLUSIVE OR, B = A

$$P = (P_{t-1}) \cdot (\bar{A} + \bar{C}) \cdot \bar{\phi}_x + (A\bar{C} + \bar{A}C) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_C	2	600	600
C_B	3	190	190
C_A	4	440	440
C_P	5	370	350
PATTERN NO.		2350	2360



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT DATA SWITCH(opt excl or)
SCALE: 0.1 mil/div		SHEET

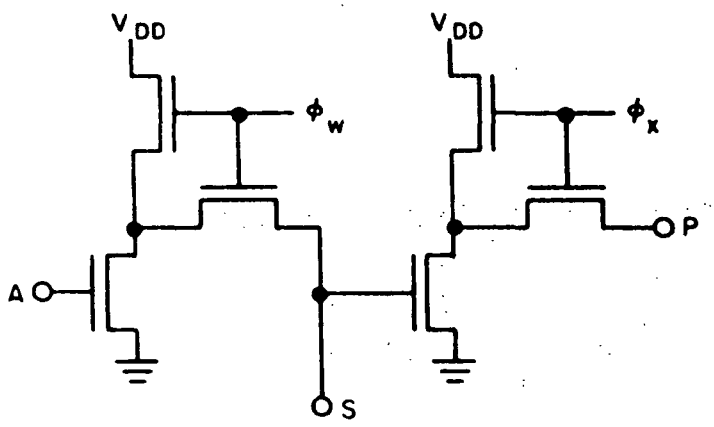
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 2pF
WITH ½ BIT AND 1 BIT DELAY OUTPUTS

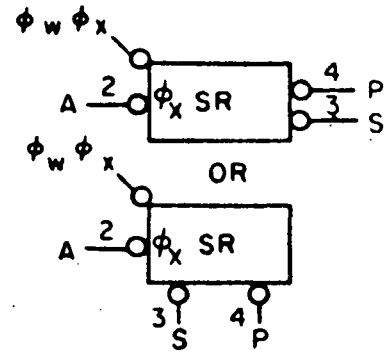
PATTERN NO. 2370 ($\phi_2\phi_1$)
2380 ($\phi_1\phi_2$)

APRIL 1968

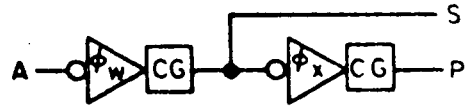
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	ϕ_w	ϕ_x	S	P
·	0	1	$\overline{A_{t-1}}$	$\overline{S_{t-1}}$
1	1	0	0	P_{t-1}
0	1	0	1	P_{t-1}

*MEANS EITHER STATE

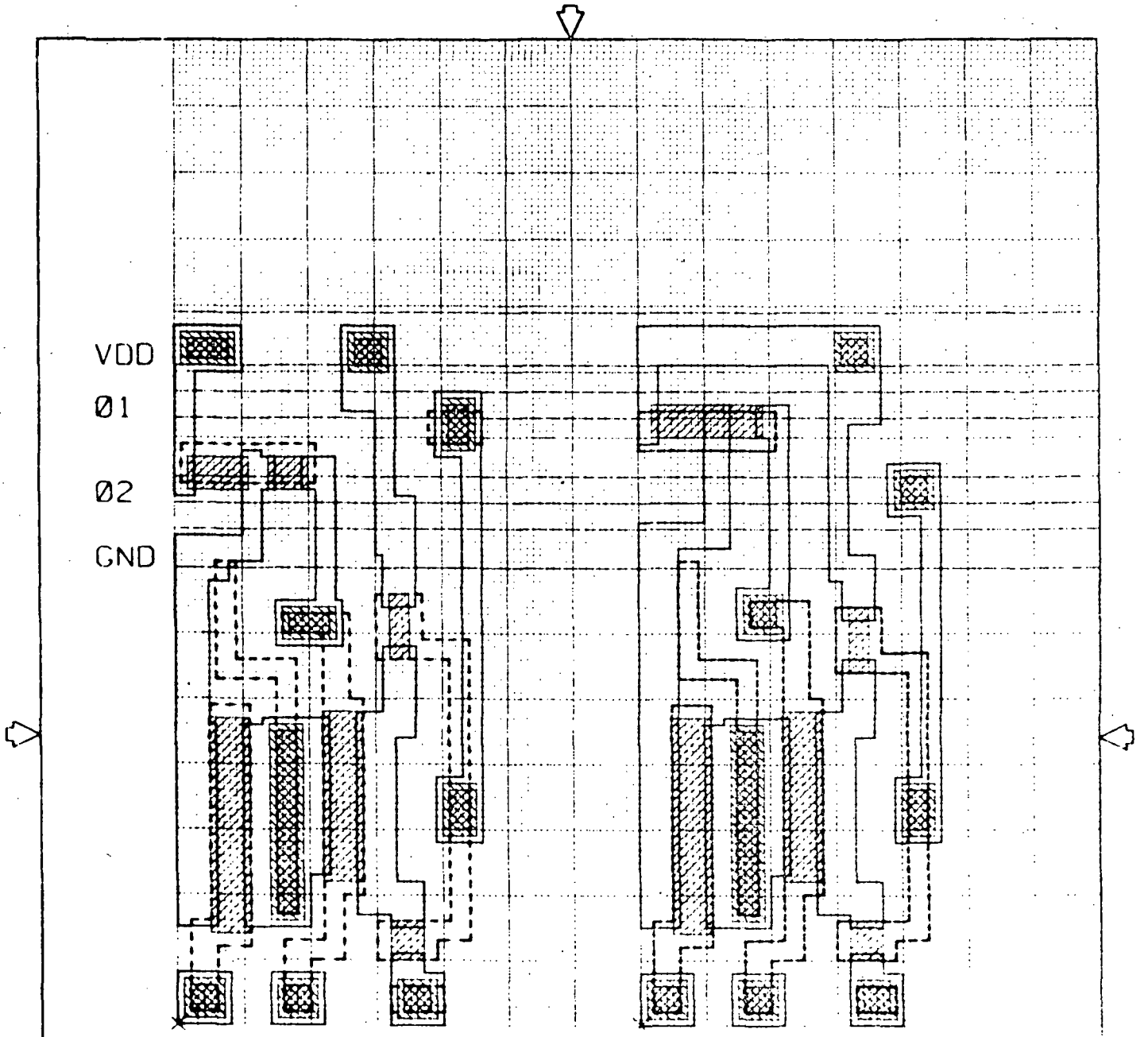
LOGIC EQUATIONS

$$S = \overline{(A_{t-1})} \cdot \phi_x + \bar{A} \cdot \phi_w$$

$$P = S_{t-1} \cdot \phi_x + P_{t-1} \cdot \phi_w$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	450	450
C_S	3	380	500
C_P	4	200	200
PATTERN NO.		2370	2380



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	DYNAMIC REGISTER STAGE Q, $\bar{Q}$ OUTPUT
SCALE 0.1mil/div		SHEET

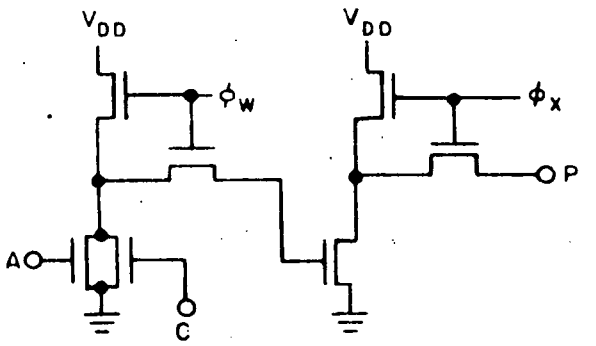
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 2pF
1 BIT DELAY OUTPUT, WITH SET

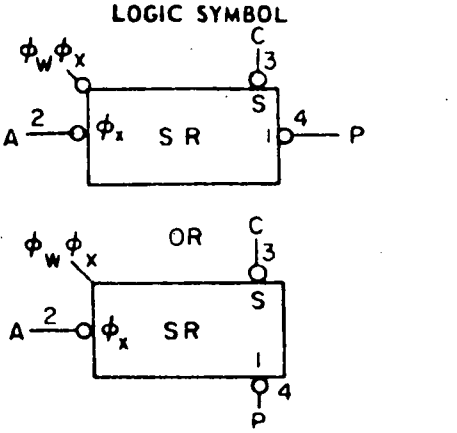
PATTERN NO. 2390 ($\phi_2\phi_1$)
2400 ($\phi_1\phi_2$)

APRIL 1968

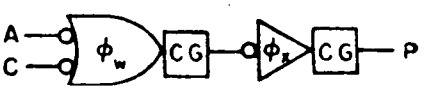
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A + C	ϕ_W	ϕ_X	P
*	0	1	$(A+C)_{t-1}$
*	1	0	P_{t-1}

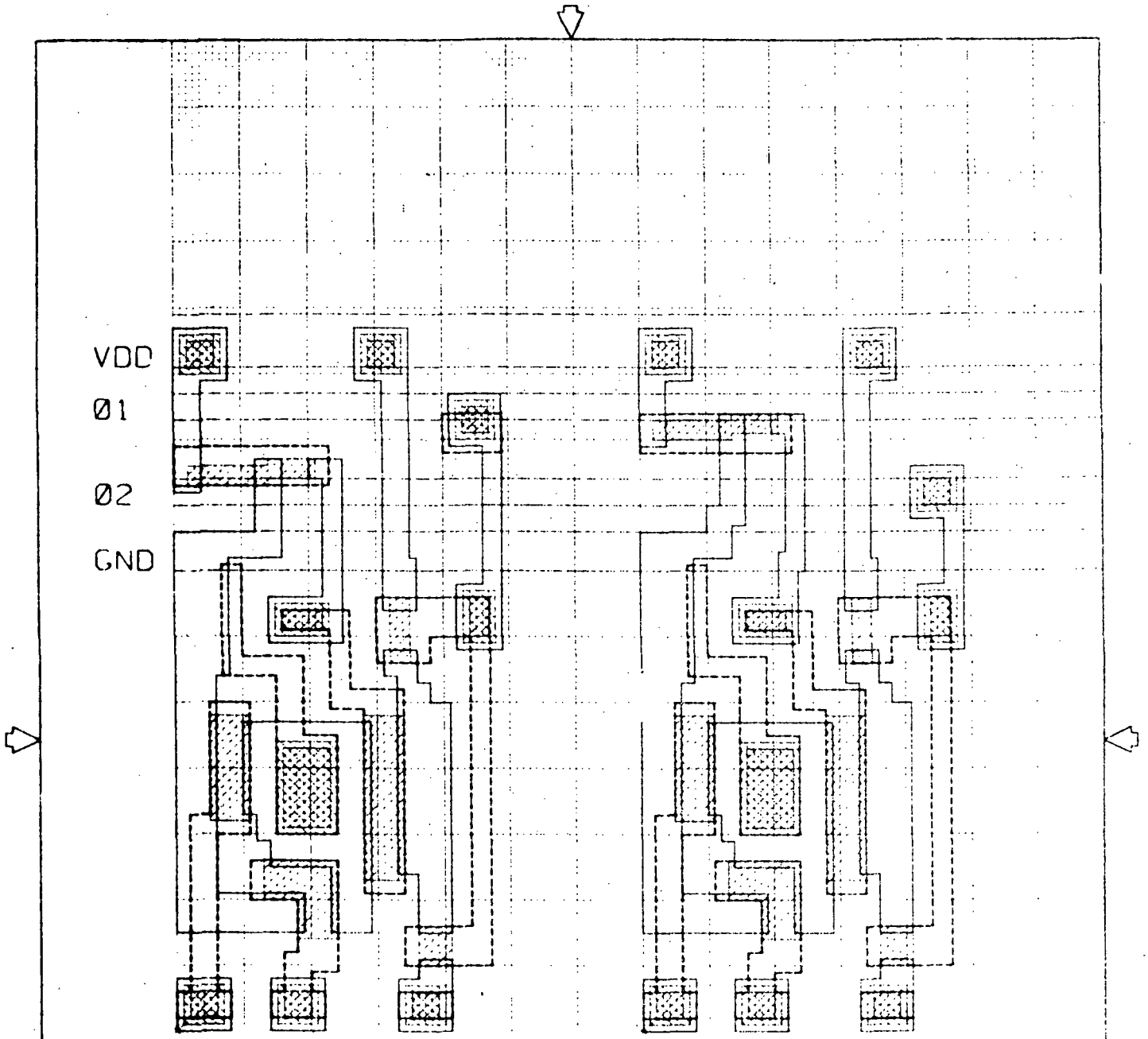
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (A + C)_{t-1} \cdot \phi_X + (P_{t-1}) \cdot \phi_W$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	260	265
C_C	3	260	265
C_P	4	210	215
PATTERN NO.		2390	2400



SIZE	CODE IDENT. NO.	DWG. NO.	DYNAMIC REGISTER Q OUTPUT W/SET
A	98230		
SCALE 0.1mil/div			SHEET

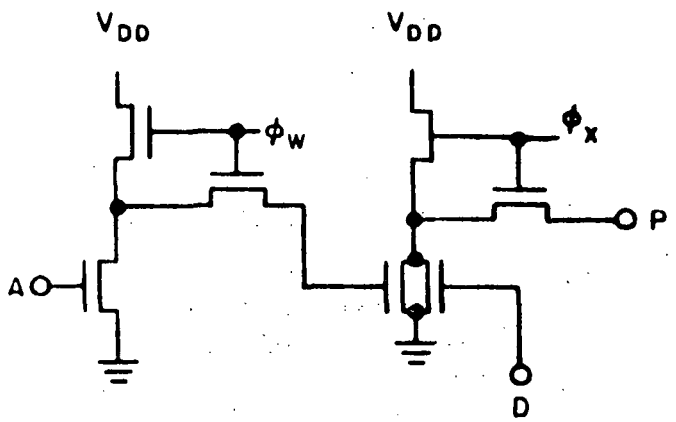
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 2pF
1 BIT DELAY OUTPUT, WITH RESET

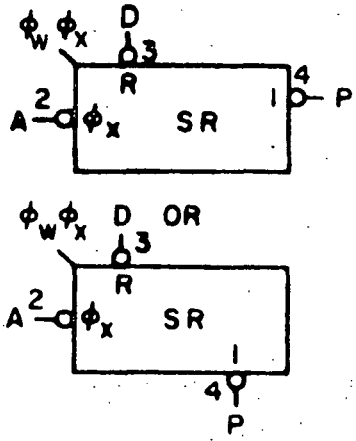
PATTERN NO. 2410 ($\phi_2\phi_1$)
2420 ($\phi_1\phi_2$)

APRIL 1968

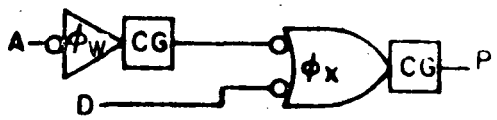
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	D	ϕ_W	ϕ_X	P
*	0	0	1	A_{t-1}
*	*	1	0	P_{t-1}
*	1	0	1	0

*MEANS EITHER STATE

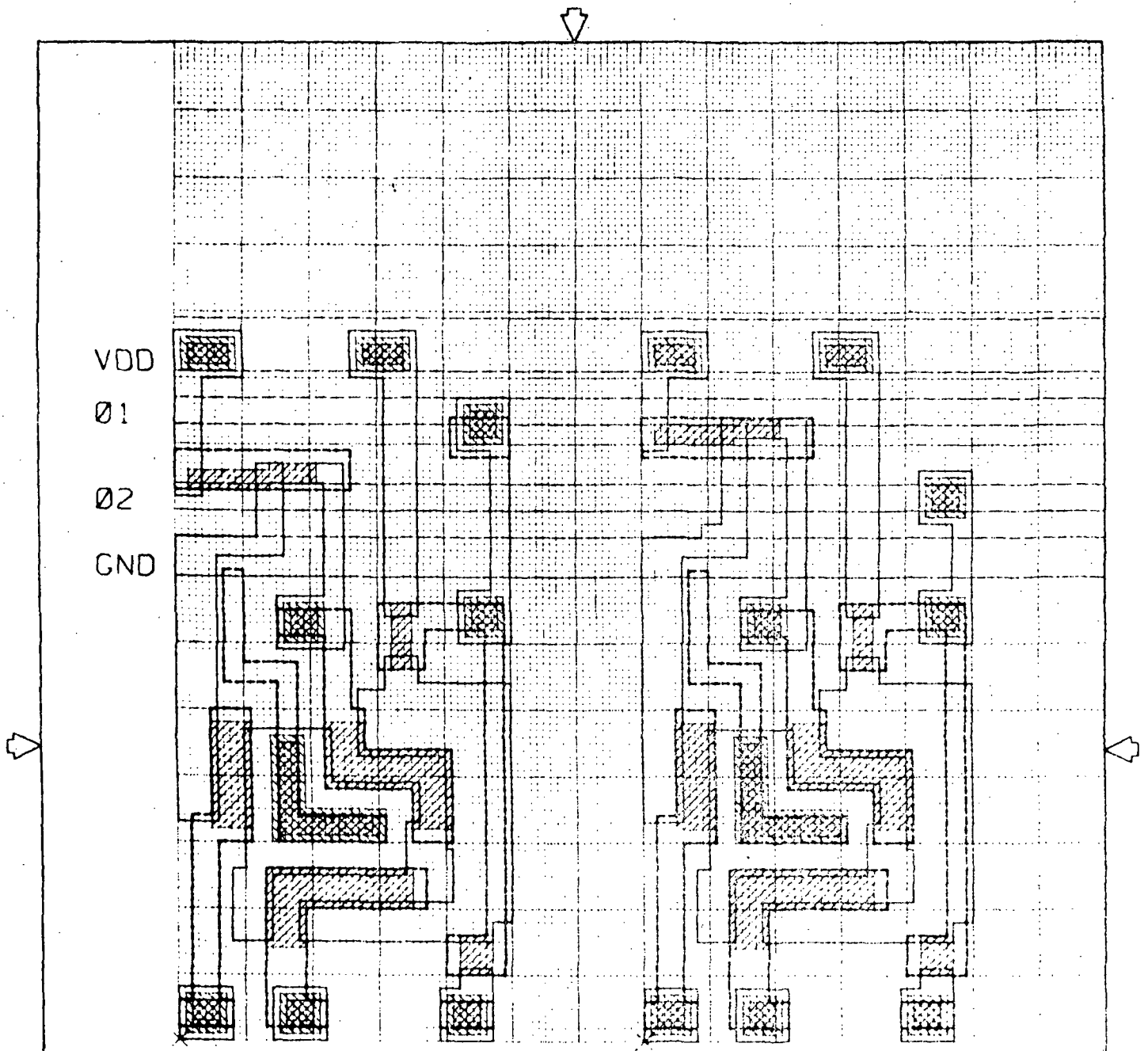
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \phi_W + (A_{t-1}) \cdot \bar{D} \cdot \phi_X$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	260	260
C_D	3	390	390
C_P	4	400	400
PATTERN NO.		2410	2420

DYNAMIC SHIFT REGISTER • 2410 2420 • APRIL 1968
1 BIT DELAY OUTPUT, WITH RESET



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	DYNAMIC REGISTER Q OUTPUT W/RESET
SCALE 0.1mil/div		SHEET

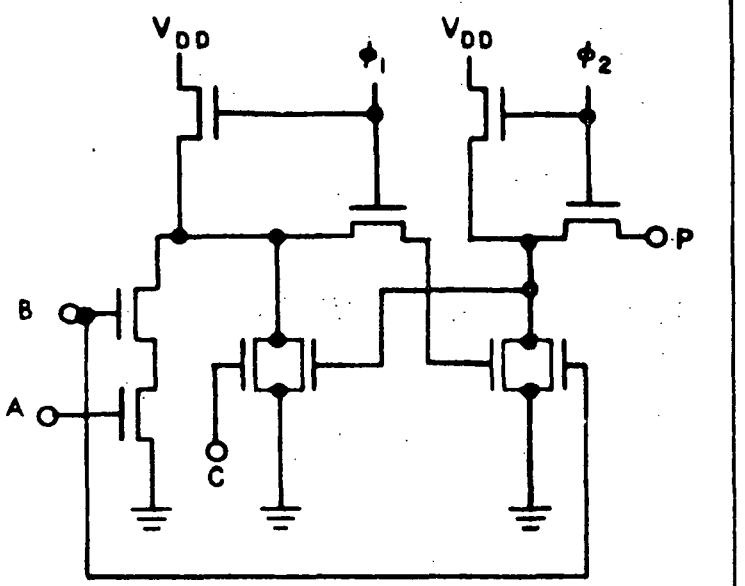
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"1" OUTPUT WITH SET

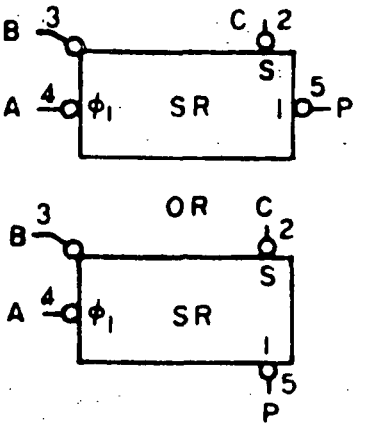
PATTERN NO. 2440 ($\phi_1 \phi_2$)

JUNE 1969

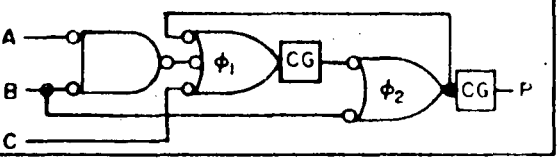
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	C_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	*	0	P_{t-1}
*	0	0	0	0	1	P_{t-1}
0	1	0	0	0	1	0
*	*	1	0	0	1	1
1	1	*	0	0	1	1

*MEANS EITHER STATE

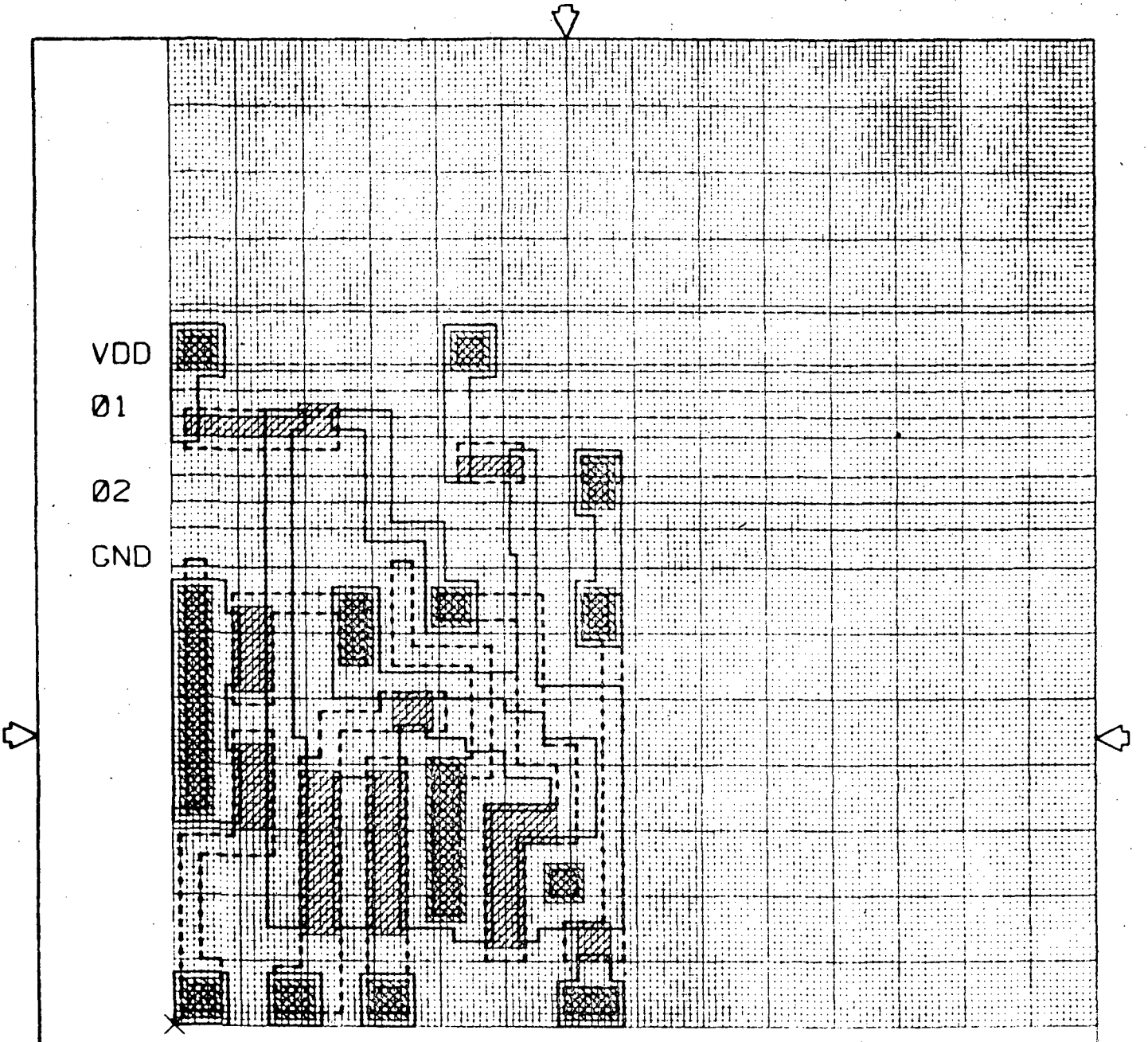
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P_t = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B} \left[A_{t-1} B_{t-1} + C_{t-1} + \overline{B_{t-1}}\ \overline{C_{t-1}}\ P_{t-1} \right]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	2	220
C_A	4	360
C_B	3	450
C_P	5	570
PATTERN NO.		2440



2440

SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REG Q OUTPUT W/SET
A	98230		
SCALE **0.1mil/div**			SHEET

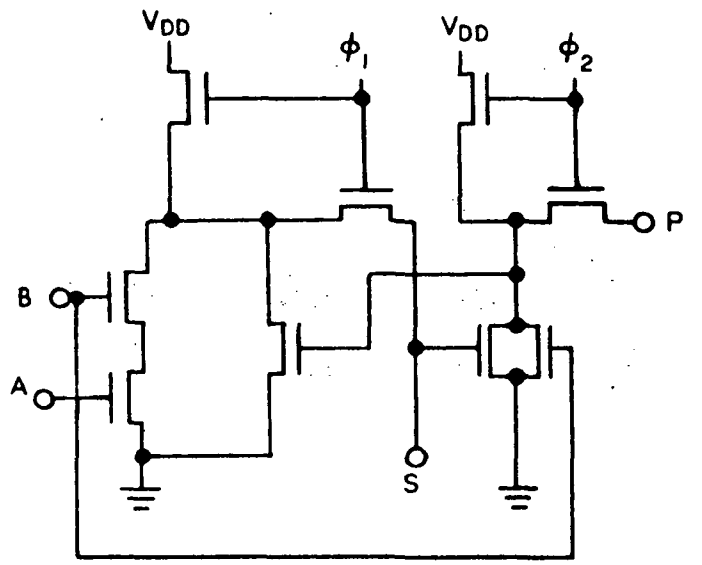
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"0" AND "1" OUTPUTS

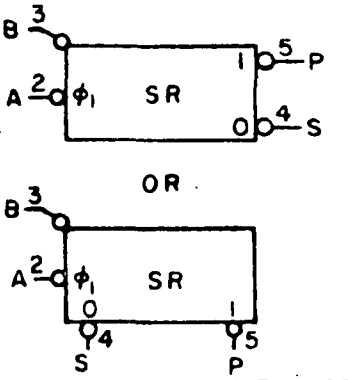
PATTERN NO. 2460 (ϕ_1 ϕ_2)

JUNE 1969

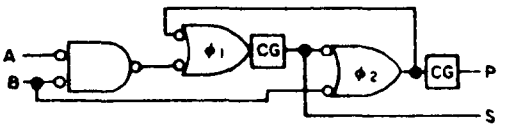
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE					
A	B	ϕ_1	S	ϕ_2	P
*	*	0	S_{t-1}	-	-
*	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	1	1	0	P_{t-1}
1	1	1	0	0	P_{t-1}
*	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	0	1	1	0
*	0	0	0	1	1
*MEANS EITHER STATE					

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

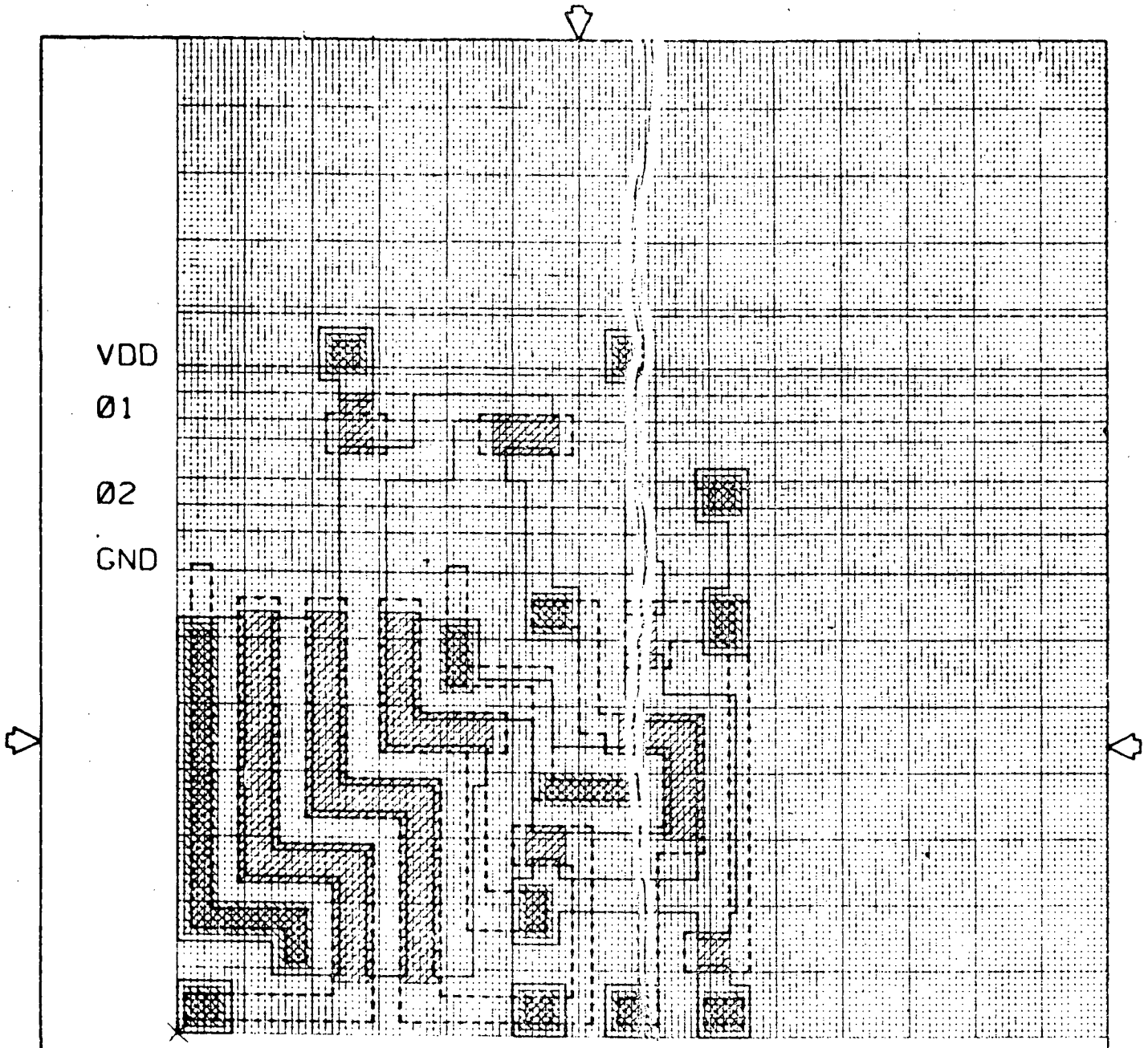
LOGIC EQUATIONS

$$S = [\bar{B} \cdot \overline{P_{t-1}} + \bar{A} \cdot B]\,\phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

$$P = \overline{S_{t-1}} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$= [\overline{B_{t-1}} \cdot P_{t-1} + A_{t-1} \cdot B_{t-1}]\,\phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES		
CAPACITOR	PIN	CAPACITY IN fF
C_A	2	910
C_B	3	1000
C_S	4	910
C_P	5	620
PATTERN NO.		2460



SIZE	CODE IDEN. NO.	DWG. NO.	STATIC REGISTER Q, $\bar{Q}$ OUTPUT
A	98230		
SCALE 0.1 mil/div			SHEET

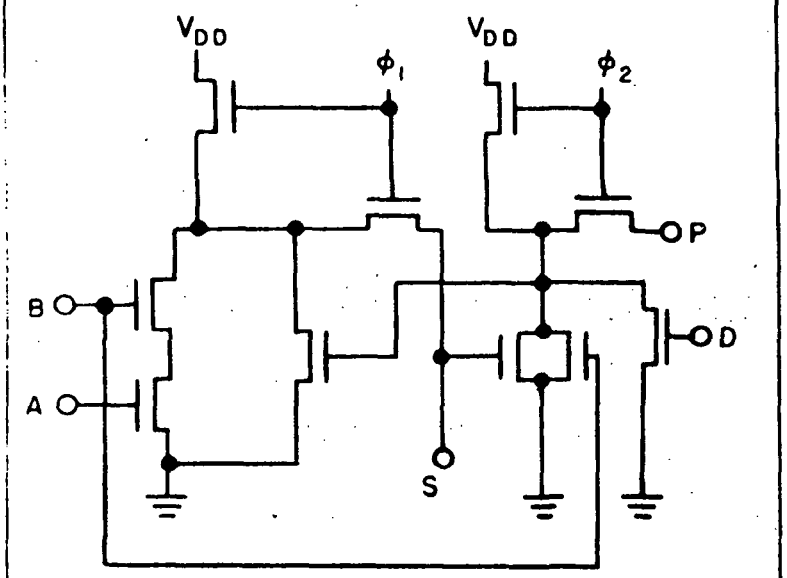
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"0" AND "1" OUTPUTS WITH RESET

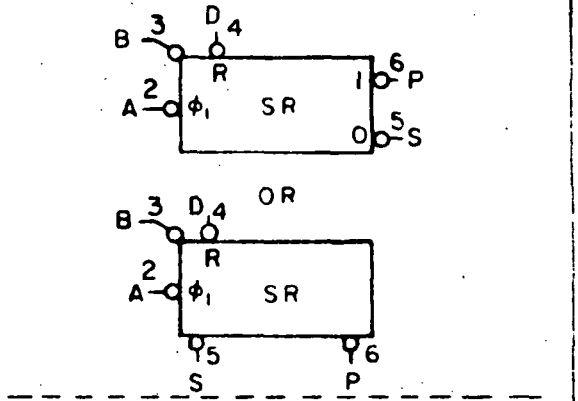
PATTERN NO. 2480 (ϕ_1, ϕ_2)

JUNE 1969

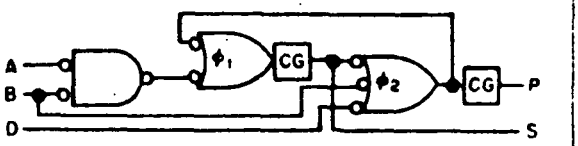
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	D	ϕ_1	S	ϕ_2	P
*	*	*	0	S_{t-1}	–	–
*	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
*	0	1	1	1	0	P_{t-1}
0	*	1	1	1	0	P_{t-1}
0	1	*	1	1	0	P_{t-1}
1	1	*	1	0	0	P_{t-1}
*	0	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	1	0	*	1	0
*	0	0	0	1	1	0
*	0	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

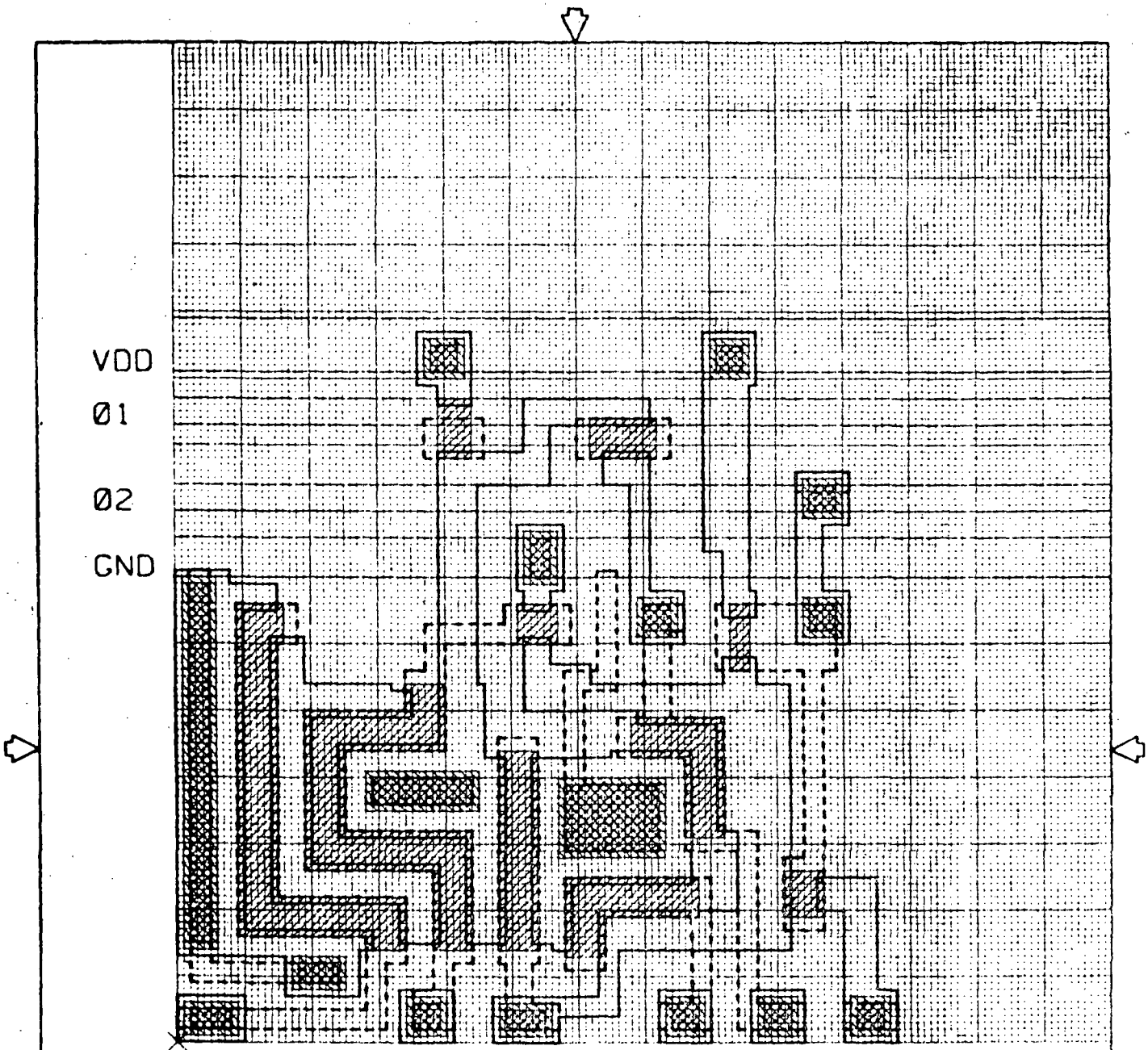
$$S = [(\bar{A} + \bar{B}) \cdot D + B \cdot \bar{A} + \bar{B} \cdot \bar{D} \cdot \overline{P_{t-1}}] \cdot \phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \overline{\phi_2}$$

$$= [A_{t-1} \cdot B_{t-1} + \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	930
C_B	3	1030
C_D	4	370
C_S	5	950
C_P	6	840
PATTERN NO.		2480



2480

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	STATIC REGISTER Q, $\bar{Q}$ OUTPUT W/RESET	
SCALE 0.1mil/div			SHEET

BANNING THICK OXIDE STANDARD CELL

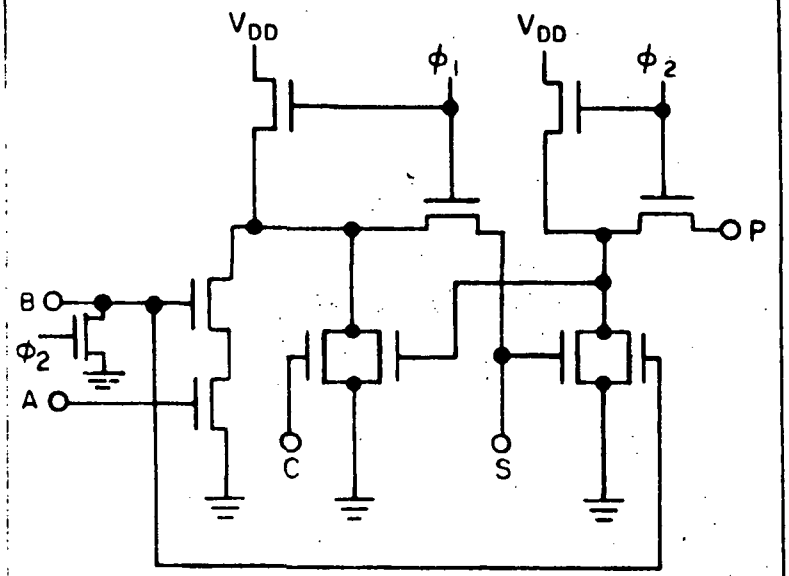
STATIC REGISTER, 2pF

PATTERN NO. 2500 (ϕ_1 ϕ_2)

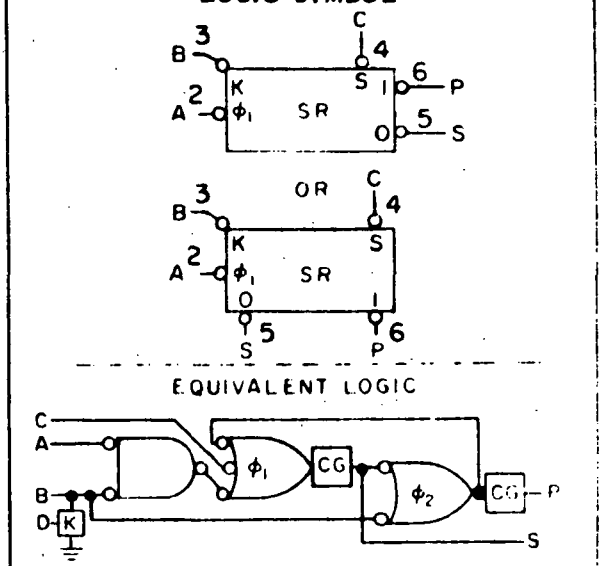
"0" AND "1" OUTPUTS, SET AND KILL

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC

TRUTH TABLE

A	B	C	ϕ_1	S	ϕ_2	P
·	·	·	0	S_{t-1}	–	–
·	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	0	1	1	0	P_{t-1}
·	·	1	1	0	0	P_{t-1}
1	1	·	1	0	0	P_{t-1}
·	0	·	0	$\overline{P_{t-1}}$	1	P_{t-1}
·	0	·	0	1	1	0
·	0	·	0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

$$S \quad [\bar{B} \cdot \bar{C} \cdot \overline{P_{t-1}} + B \cdot \bar{A} \cdot \bar{C}] \cdot \phi_1 + S_{t-1} \cdot \overline{\phi_1}$$

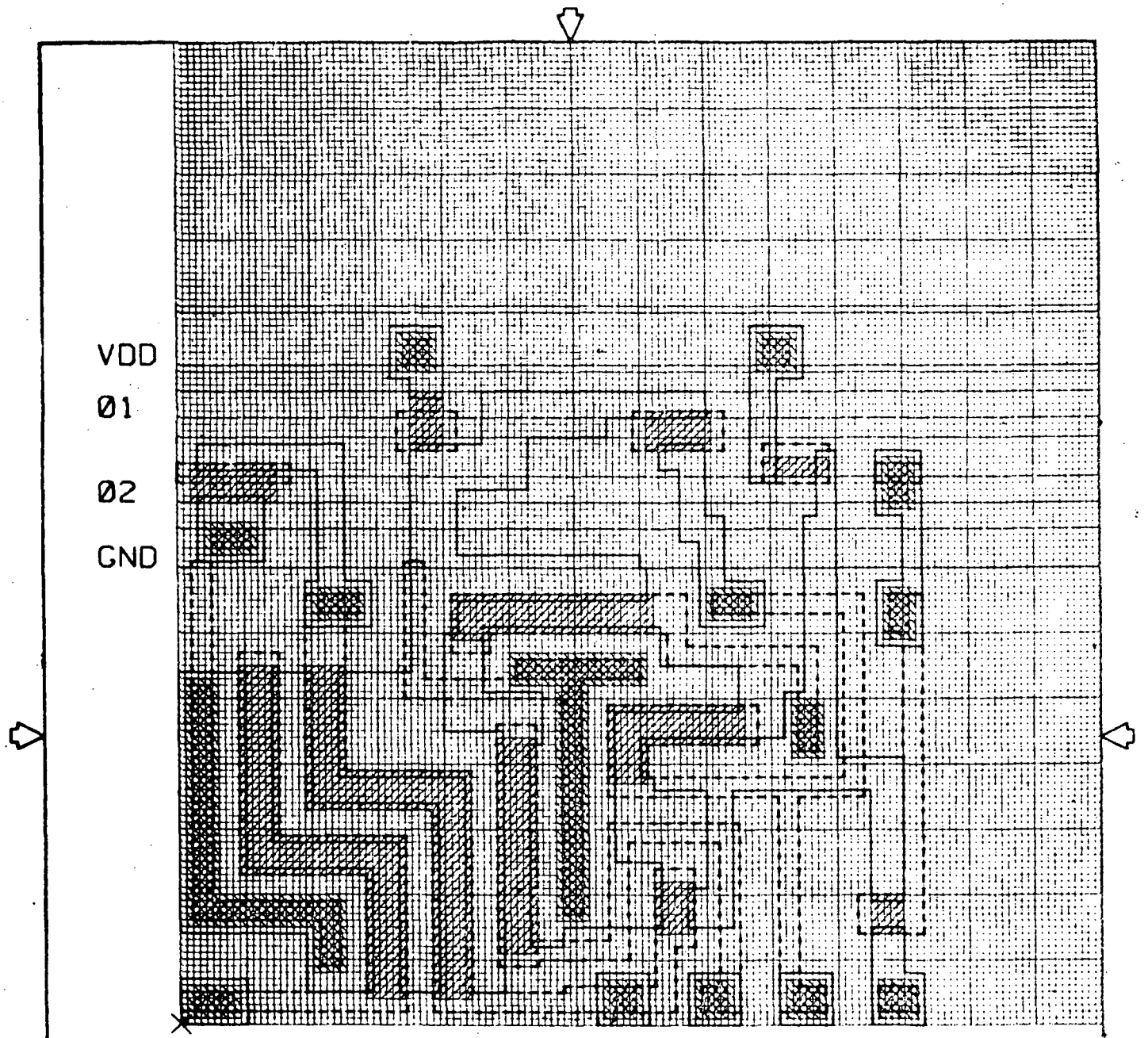
$$P \quad \overline{S_{t-1}} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

$$[A_{t-1} \cdot B_{t-1} + C_{t-1} + \overline{B_{t-1}} \cdot \overline{C_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B}$$

$$+ P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	4	490
C_A	2	910
C_B	3	1180
C_S	5	1210
C_P	6	740
PATTERN NO.		2500



SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REGISTER Q, $\bar{Q}$ OUTPUT W/SET AND KILL
A	98230		
SCALE 0.1mil/div			SHEET

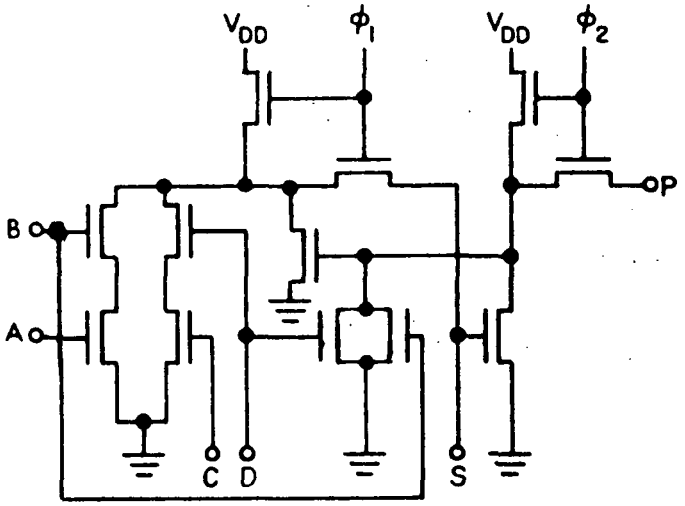
BANNING THICK OXIDE STANDARD CELL

DUAL SAMPLE REGISTER, 2pF
"0" AND "1" OUTPUTS

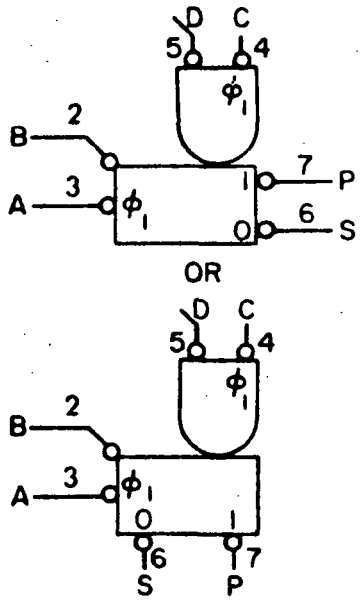
PATTERN NO. 2520 (ϕ_1 ϕ_2)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

J	K	ϕ_1	S	D	ϕ_2	P
*	*	0	S_{t-1}	–	–	–
0	0	1	$\overline{P_{t-1}}$	0	0	P_{t-1}
1	0	1	1	*	0	P_{t-1}
*	1	1	0	*	0	P_{t-1}
0	*	0	$\overline{P_{t-1}}$	0	1	P_{t-1}
1	*	0	*	1	1	0
0	*	0	1	0	1	0
0	0	0	0	0	1	1

*MEANS EITHER STATE

B AND D ARE SAMPLE INPUTS
DURING ϕ_2 B AND D MUST EQUAL ZERO

LOGIC EQUATIONS

J = B + D

K = A · B + C · D

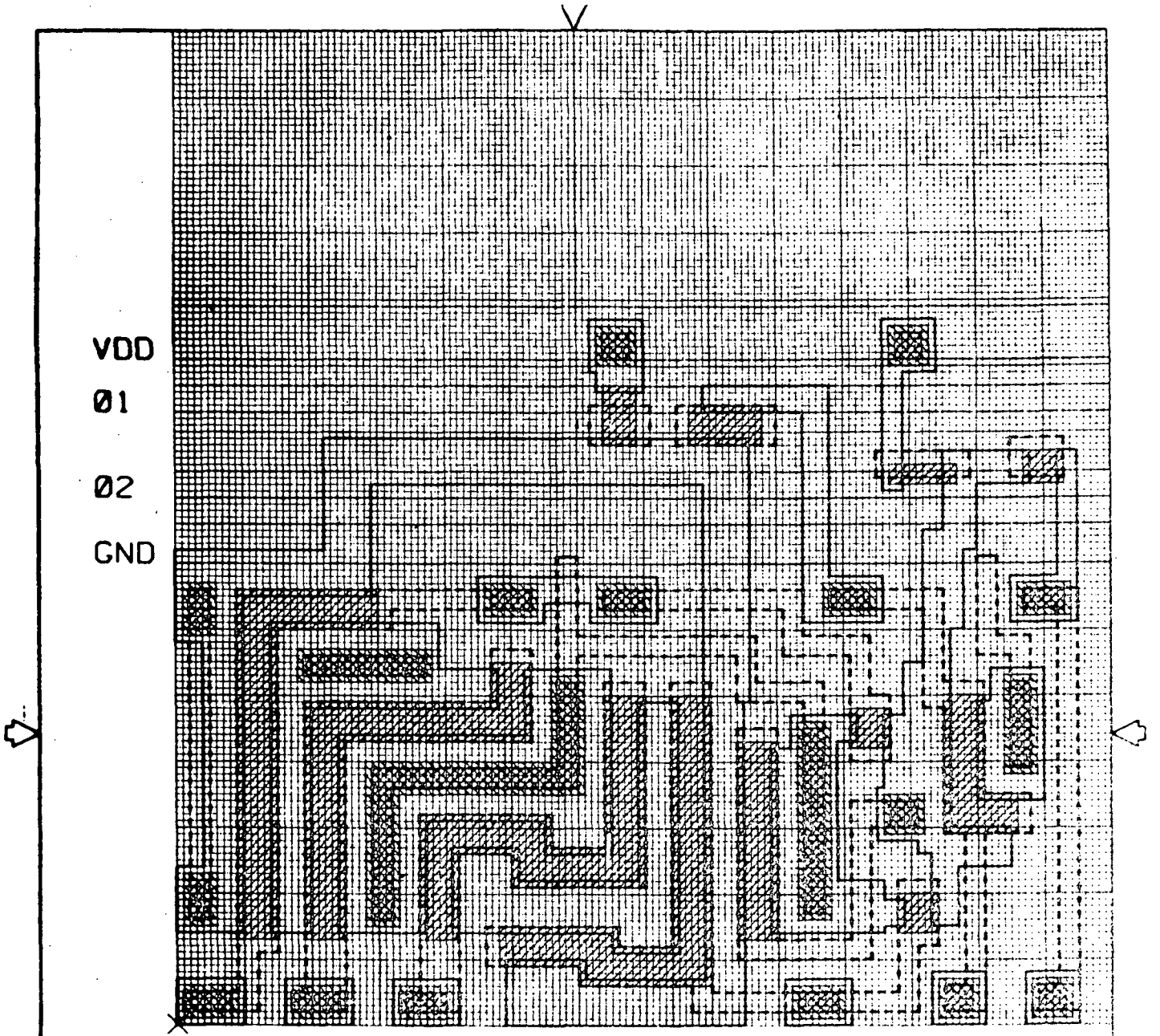
$$S = S_{t-1} \cdot \bar{\phi}_1 + [J \cdot \bar{K} + \bar{J} \cdot \bar{K} \cdot \overline{P_{t-1}}] \cdot \phi_1$$

$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \bar{B} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$= [K_{t-1} + \overline{J_{t-1}} \cdot \overline{K_{t-1}} \cdot P_{t-1}] \cdot \bar{D} \cdot \bar{B} \cdot \bar{\phi}_2 + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	900
C_B	2	1110
C_C	4	960
C_D	5	1030
C_S	6	1570
C_P	7	760
PATTERN NO.		2520



2520

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	DUAL SAMPLE REGISTER Q, $\bar{Q}$ OUT
SCALE 0.1mil/div		SHEET

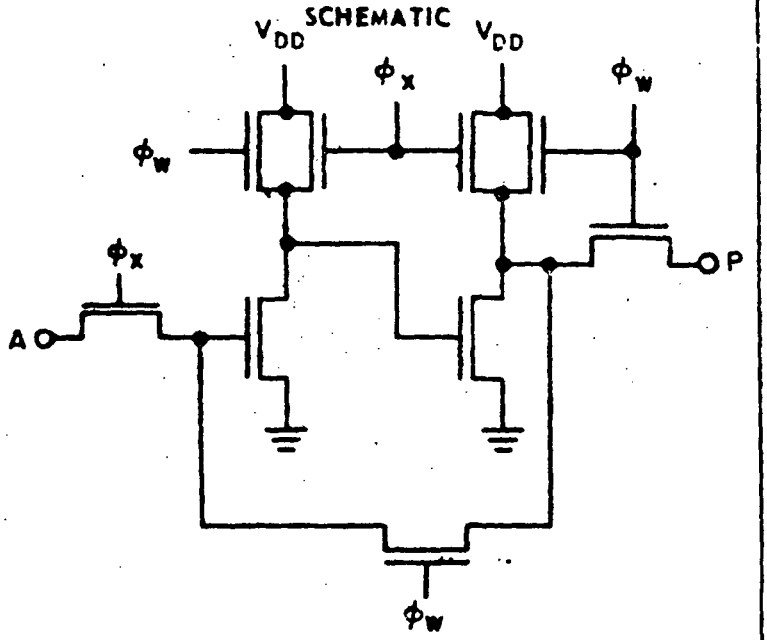
BANNING THICK OXIDE STANDARD CELL

SCHMITT TRIGGER

PATTERN NO. 2560 [ϕ_2]
2570 [ϕ_1]

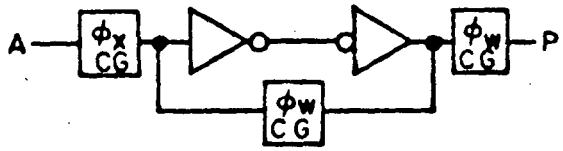
JANUARY 1969

SCHEMATIC



LOGIC SYMBOL

EQUIVALENT LOGIC



TRUTH TABLE

A	ϕ_w	P
*	0	A_{t-1}
0	1	0
1	1	1

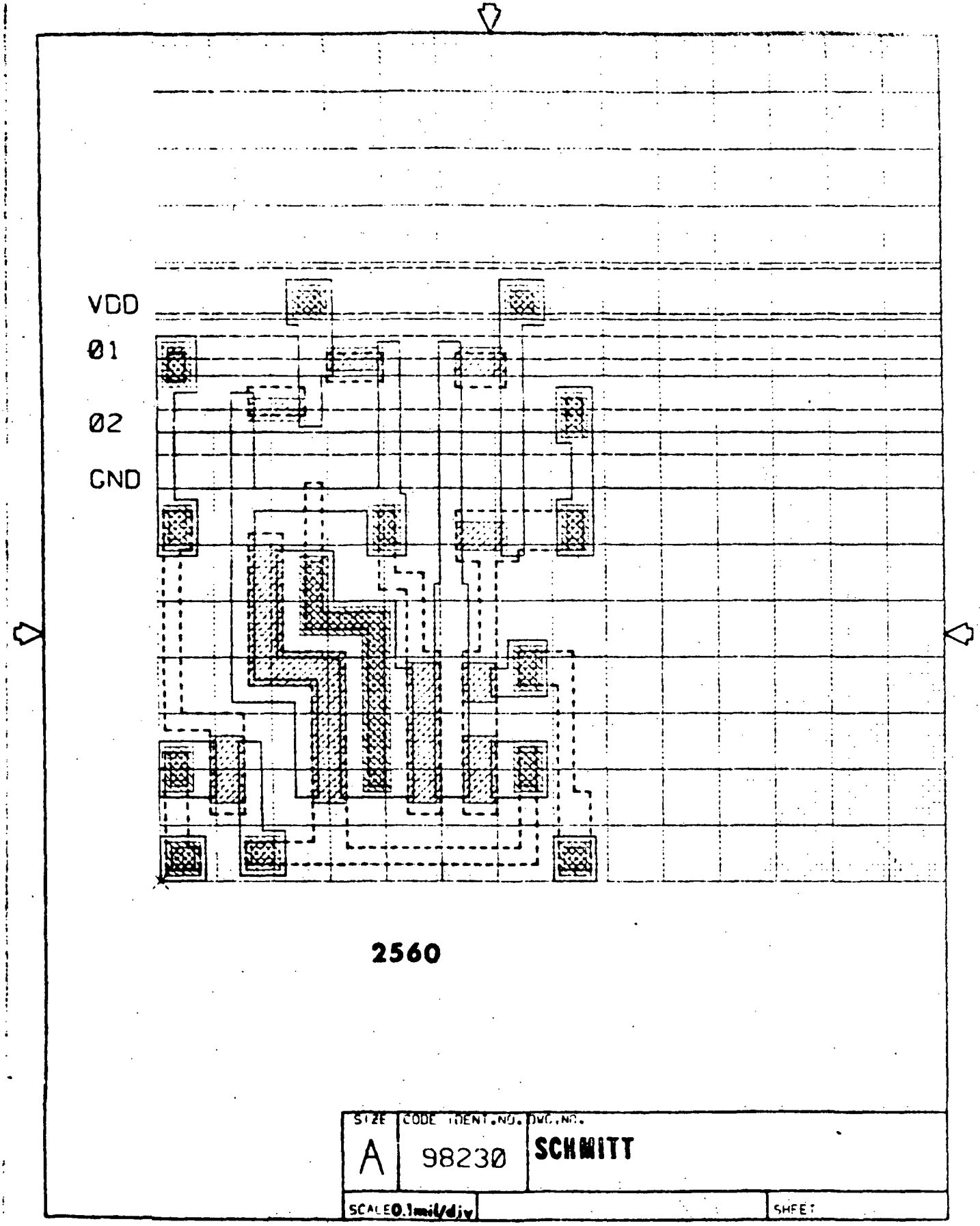
*MEANS EITHER STATE

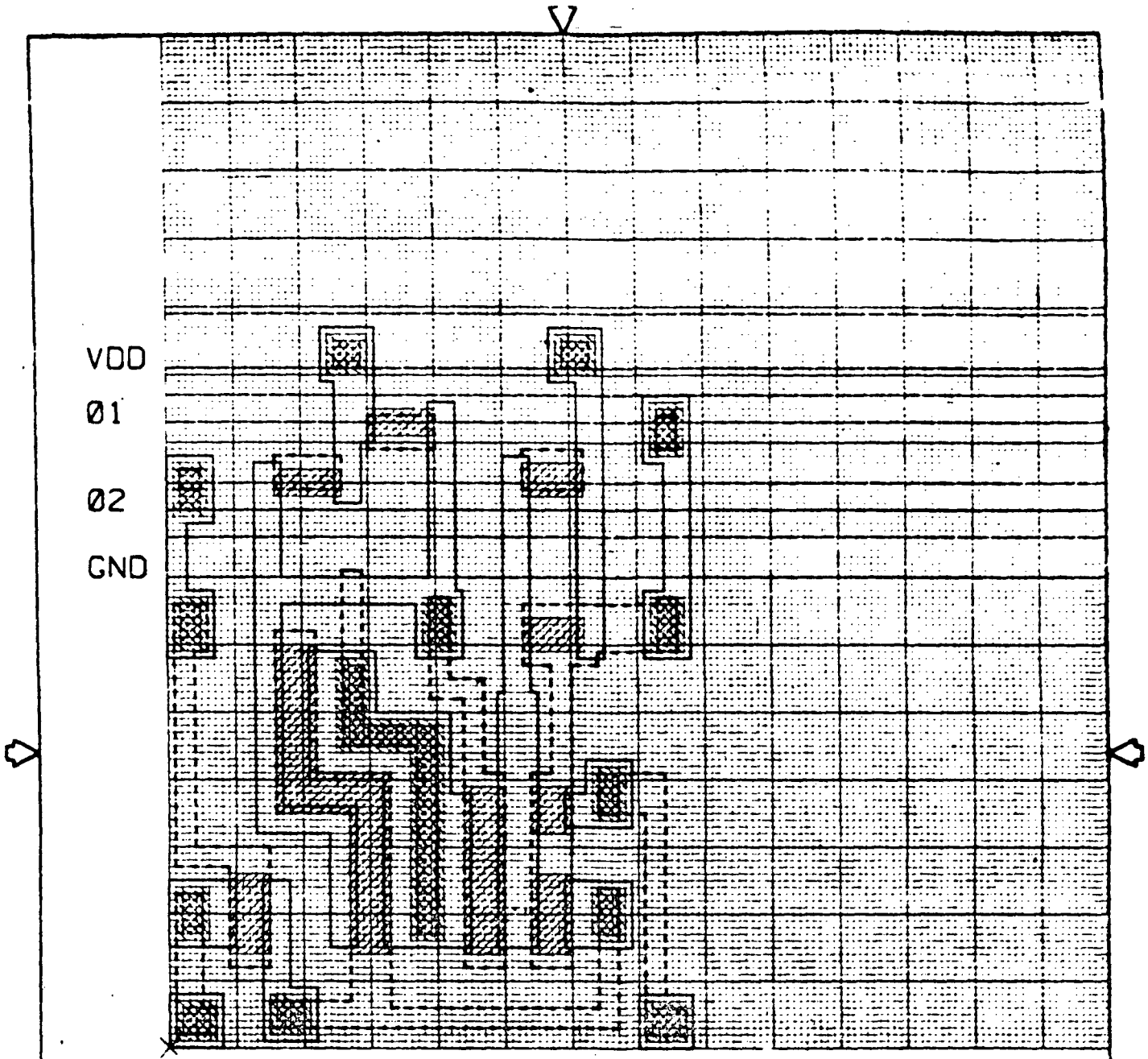
LOGIC EQUATIONS

$$P = (A_{t-1}) \cdot \bar{\phi}_w \cdot A \cdot \phi_w$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	1010	1010
C_P	3	130	130
PATTERN NO.		2560	2570


VDD
Ø1
Ø2
GND
2560
SIZE
A
CODE IDENT.NO.
98230
DWG.NO.
SCHMITT
SCALE 0.1mil/div
SHEET



2570

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	SCHMITT
SCALE		SHEET

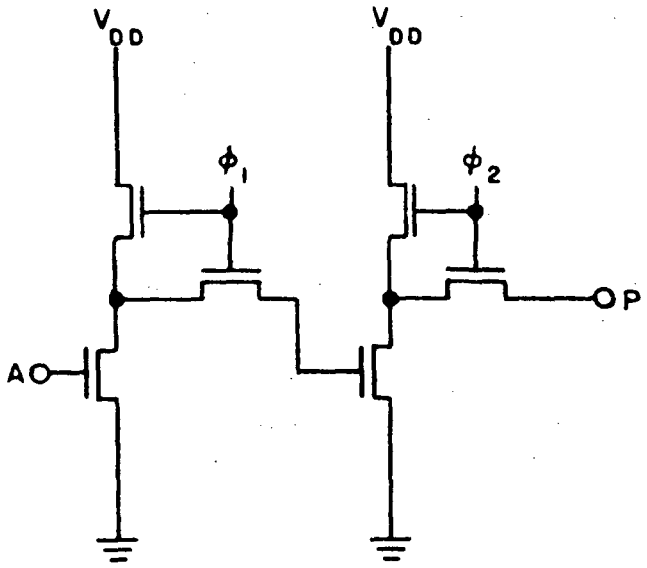
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 2pF
1 BIT DELAY OUTPUT

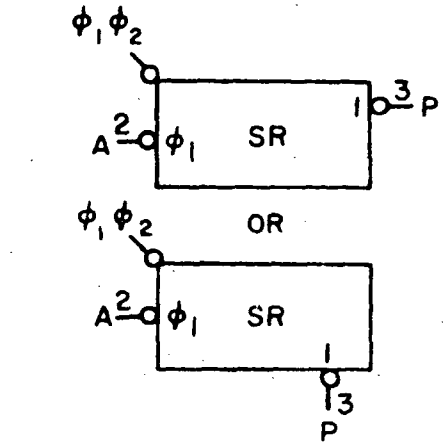
PATTERN NO. 2580 (ϕ_1 ϕ_2)

APRIL 1969

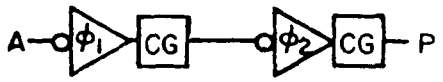
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	ϕ_1	ϕ_2	P
*	0	1	A_{t-1}
*	1	0	P_{t-1}

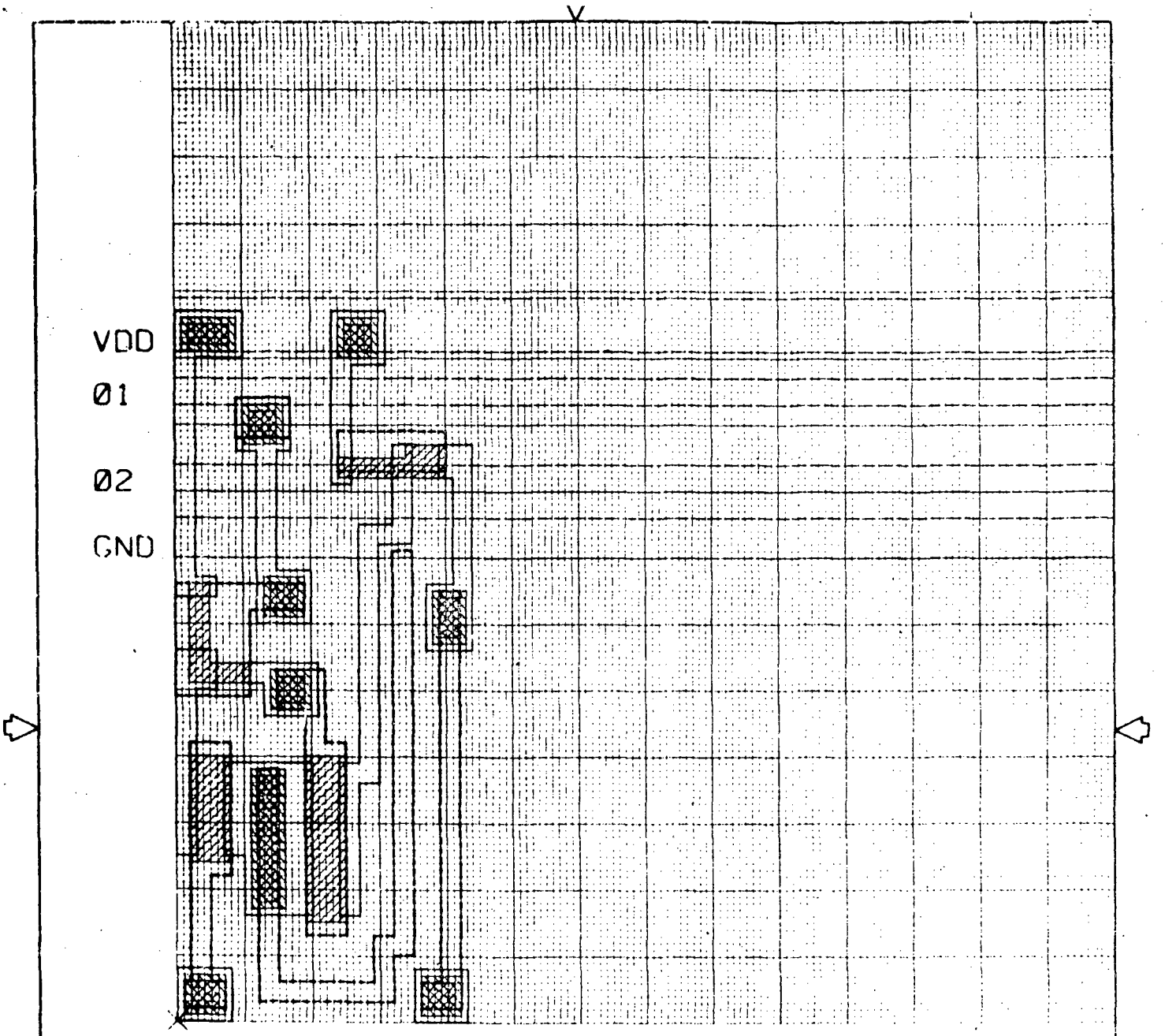
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (A_{t-1}) \cdot \phi_2 + (P_{t-1}) \cdot \phi_1$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	250
C_P	3	300
PATTERN NO.		2580



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	SR, Q OUTPUT
SCALE 0.1 mil/div		SHEET

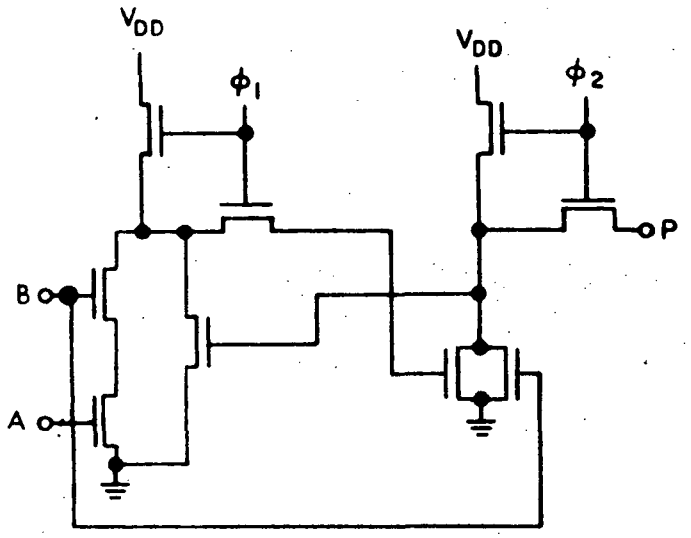
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"1" OUTPUT

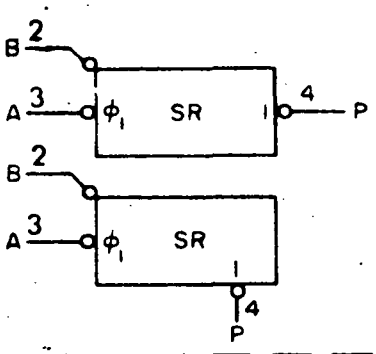
PATTERN NO. 2600 (ϕ_1 ϕ_2)

JUNE 1969

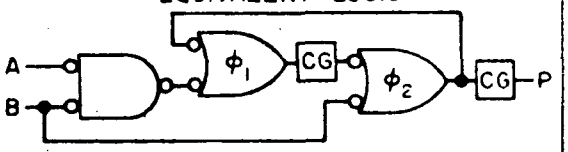
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

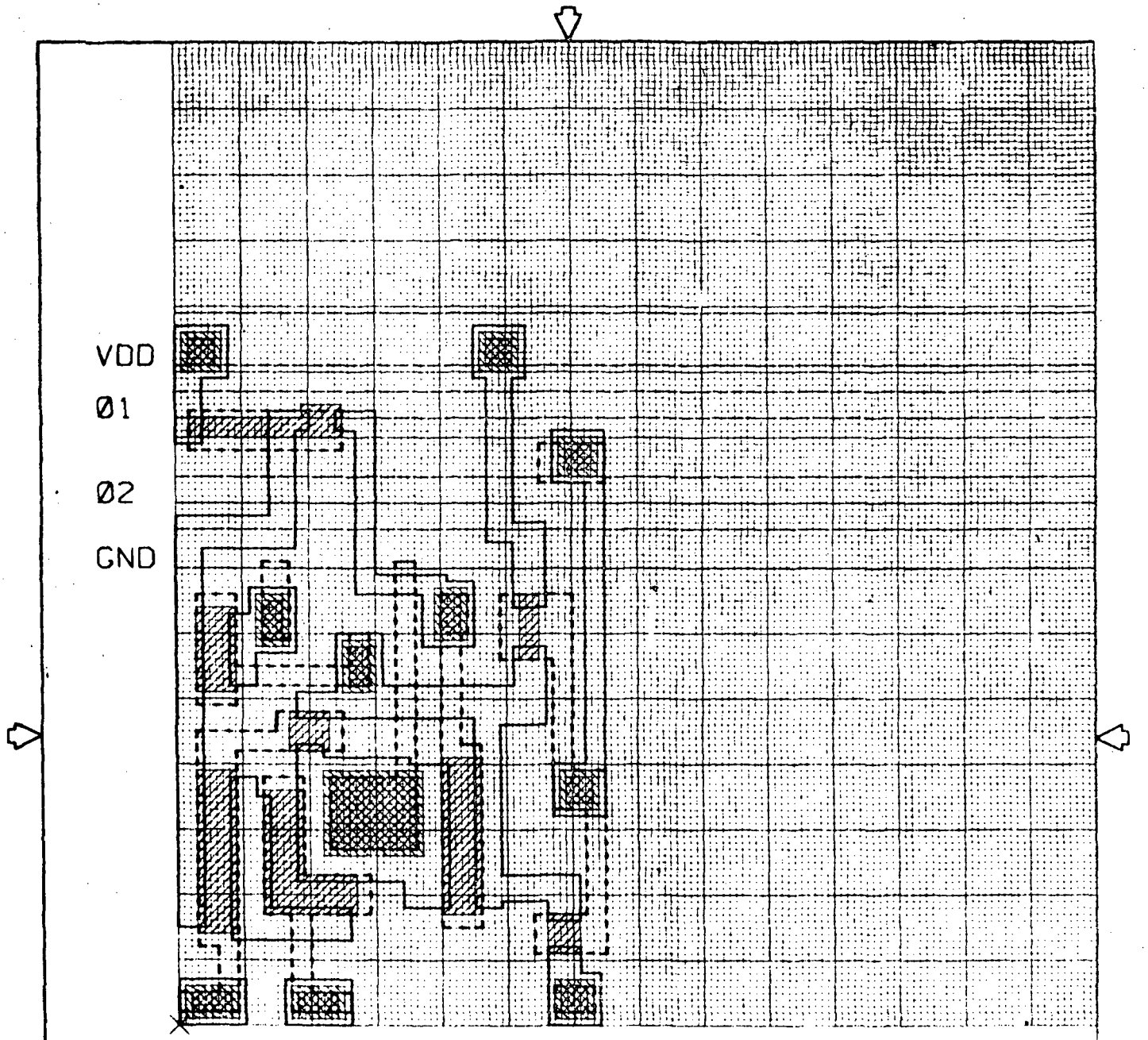
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B} \left[A_{t-1} B_{t-1} + \overline{B_{t-1}} P_{t-1} \right]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	380
C_B	2	440
C_P	4	430
PATTERN NO.		2600



2600

SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REGISTER Q, OUT
A	98230		
SCALE 0.1mil/div			SHEET

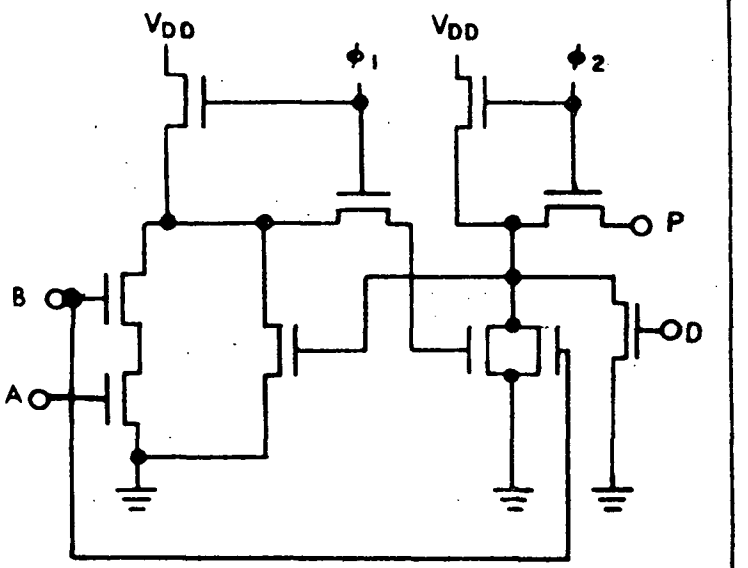
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"1" OUTPUT WITH RESET

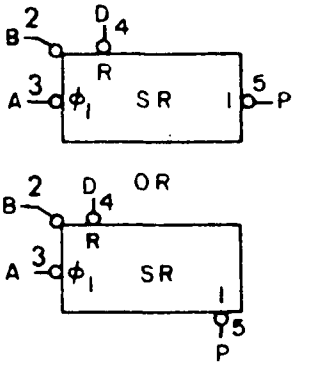
PATTERN NO. 2620 (ϕ_1 ϕ_2)

JUNE 1969

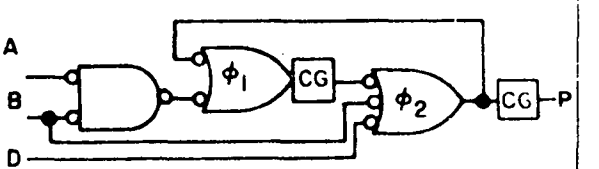
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	D_{t-1}	ϕ_1	D	B	ϕ_2	P
*	*	*	*	*	*	0	P_{t-1}
*	0	0	0	0	0	1	P_{t-1}
*	0	1	0	0	0	1	0
0	*	1	0	0	0	1	0
0	1	*	0	0	0	1	0
*	*	*	0	1	0	1	0
1	1	*	0	0	0	1	1

*MEANS EITHER STATE

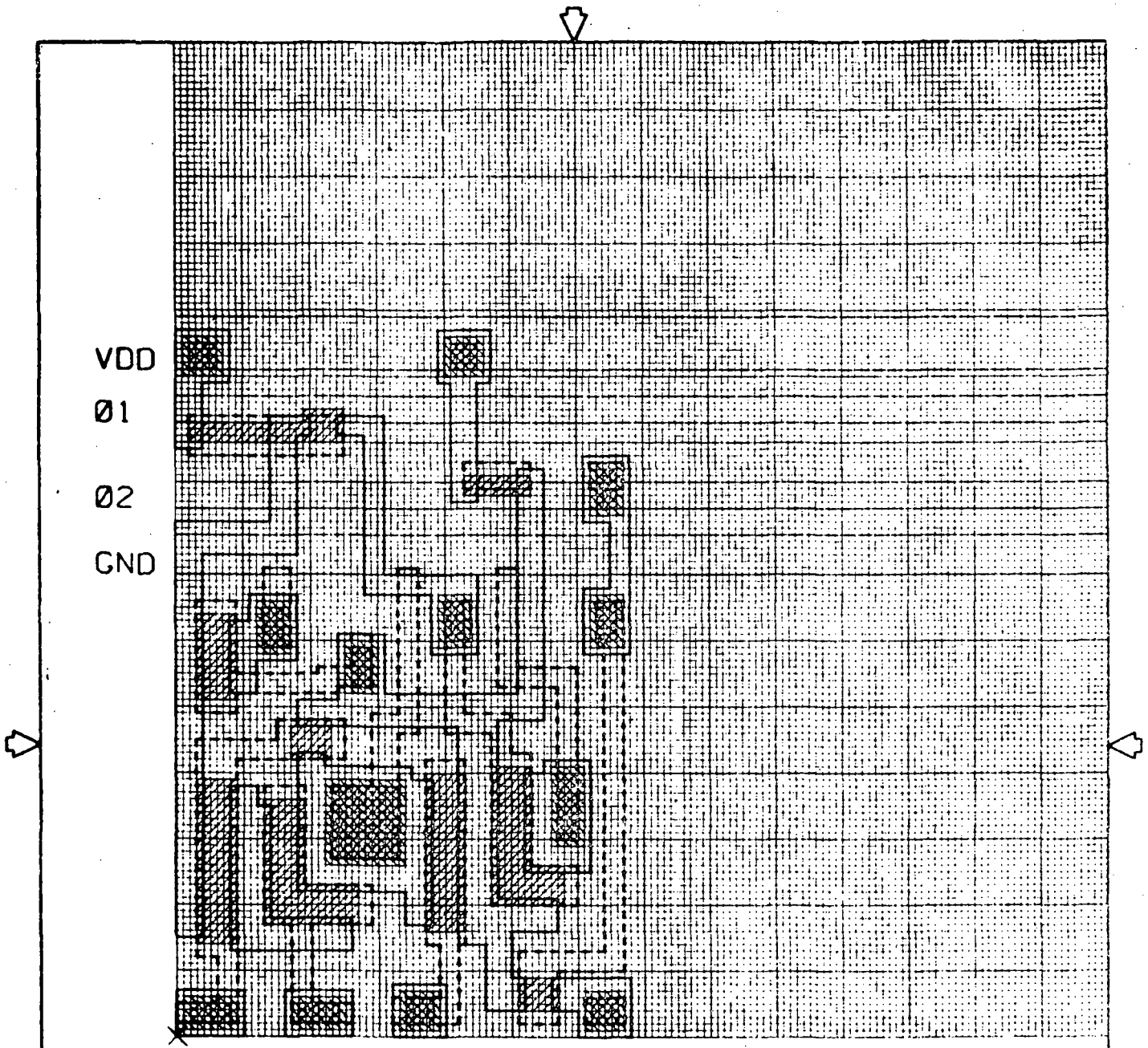
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P = [A_{t-1} \cdot B_{t-1} + \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	380
C_B	2	440
C_D	4	350
C_P	5	540
PATTERN NO.		2620



2620

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		**STATIC REGISTER Q OUTPUT W/ RESET**
SCALE **0.1mil/div**			SHEET

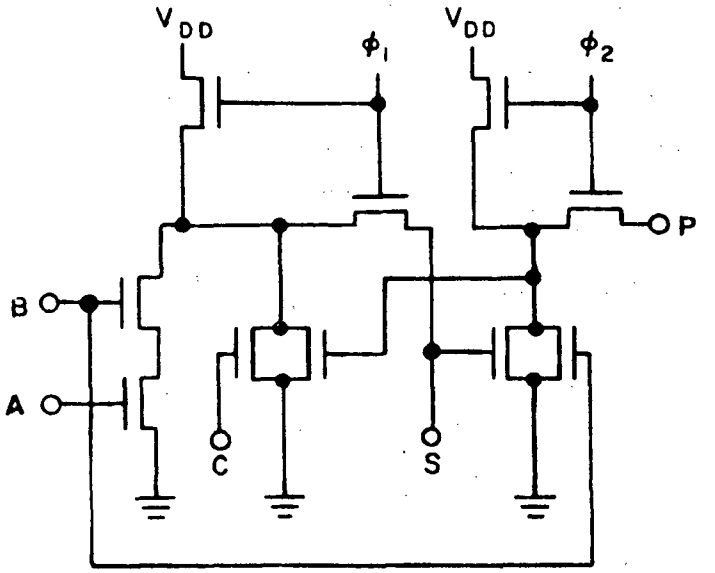
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"0" AND "1" OUTPUTS WITH SET

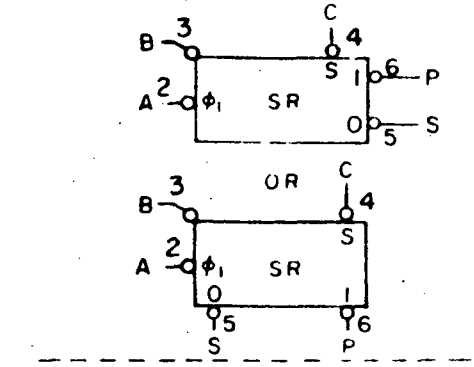
PATTERN NO. 2640 (ϕ_1 ϕ_2)

JUNE 1969

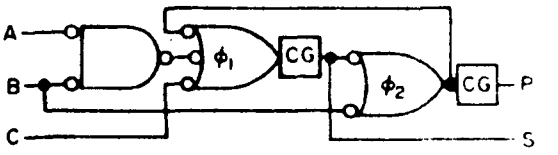
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	C	ϕ_1	S	ϕ_2	P
*	*	*	0	S_{t-1}	–	–
*	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	0	1	1	0	P_{t-1}
*	*	1	1	0	0	P_{t-1}
1	1	*	1	0	0	P_{t-1}
*	0	*	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	*	0	1	1	0
*	0	*	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

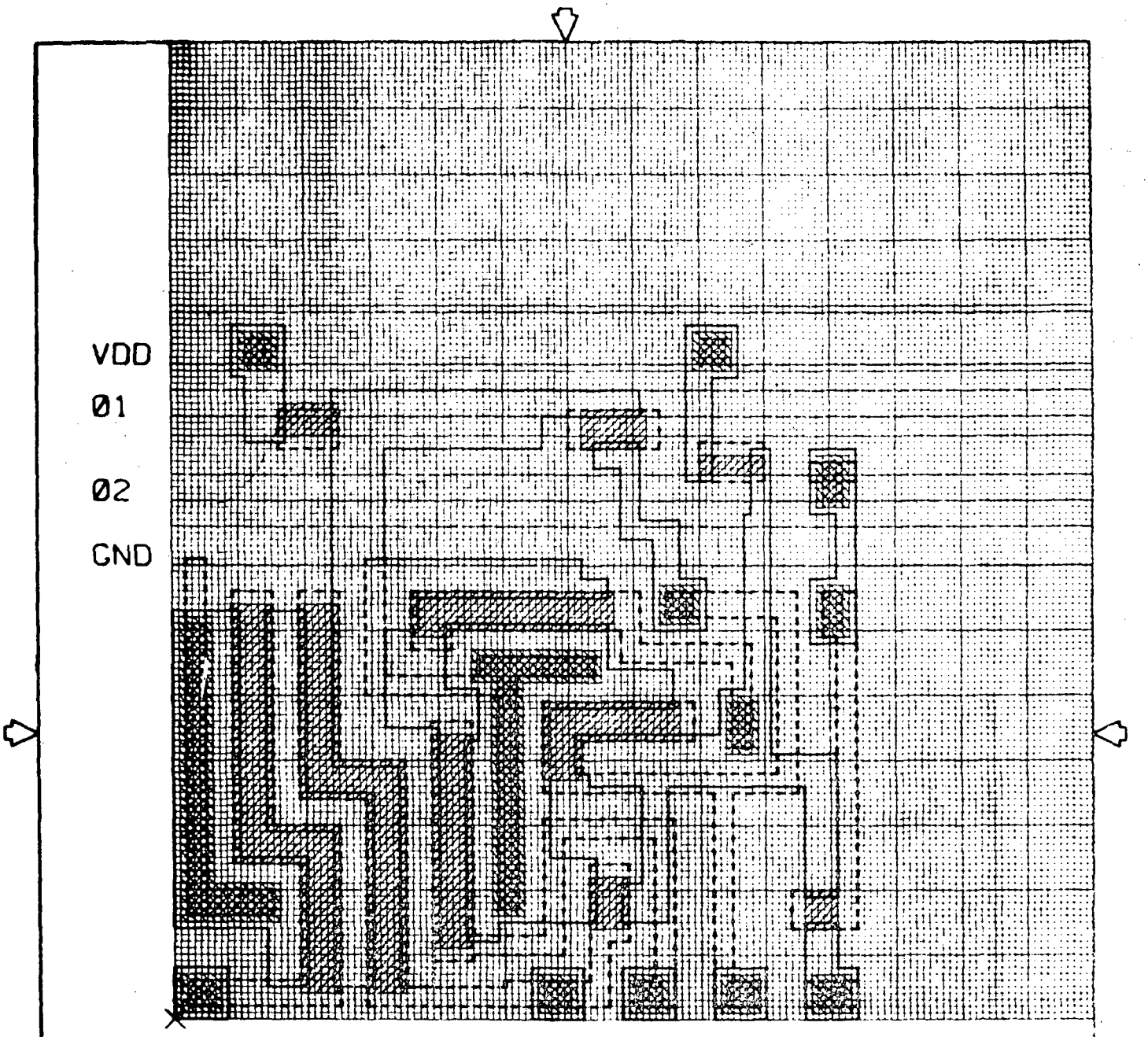
$$S = [\bar{B} \cdot \bar{C} \cdot \overline{P_{t-1}} + B \cdot \bar{A} \cdot \bar{C}] \cdot \phi_1 + S_{t-1} \cdot \overline{\phi_1}$$

$$P = \overline{S_{t-1}} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

$$= [A_{t-1} \cdot B_{t-1} + C_{t-1} + \overline{B_{t-1}} \cdot \overline{C_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	4	490
C_A	2	900
C_B	3	1010
C_S	5	1190
C_P	6	730
PATTERN NO.		2640



2640

SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REGISTER Q, $\bar{Q}$ OUTPUT W/SET
A	98230		
SCALE 0.1mil/div			SHEET

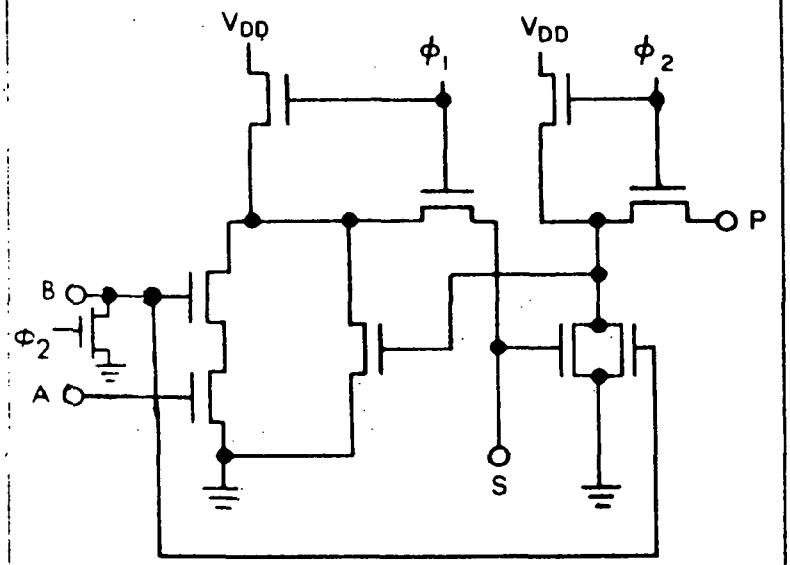
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"0" AND "1" OUTPUTS WITH KILL

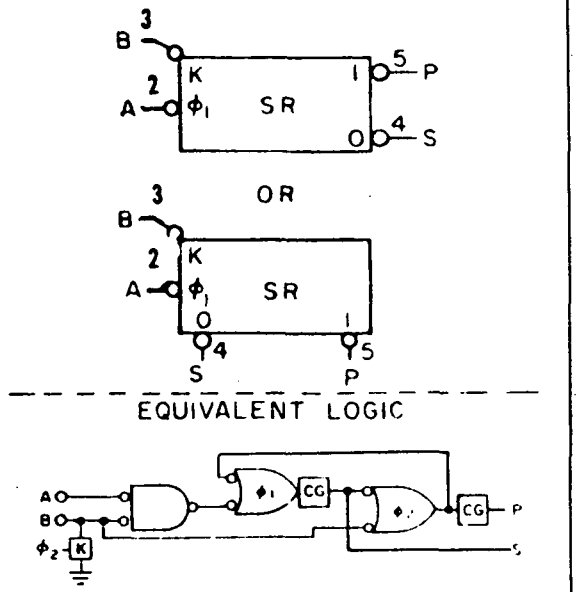
PATTERN NO. 2660 ($\phi_1\phi_2$)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_1	S	ϕ_2	P
*	*	0	S_{t-1}	-	-
*	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	1	1	0	P_{t-1}
1	1	1	0	0	P_{t-1}
*	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	0	1	1	0
*	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT

LOGIC EQUATIONS

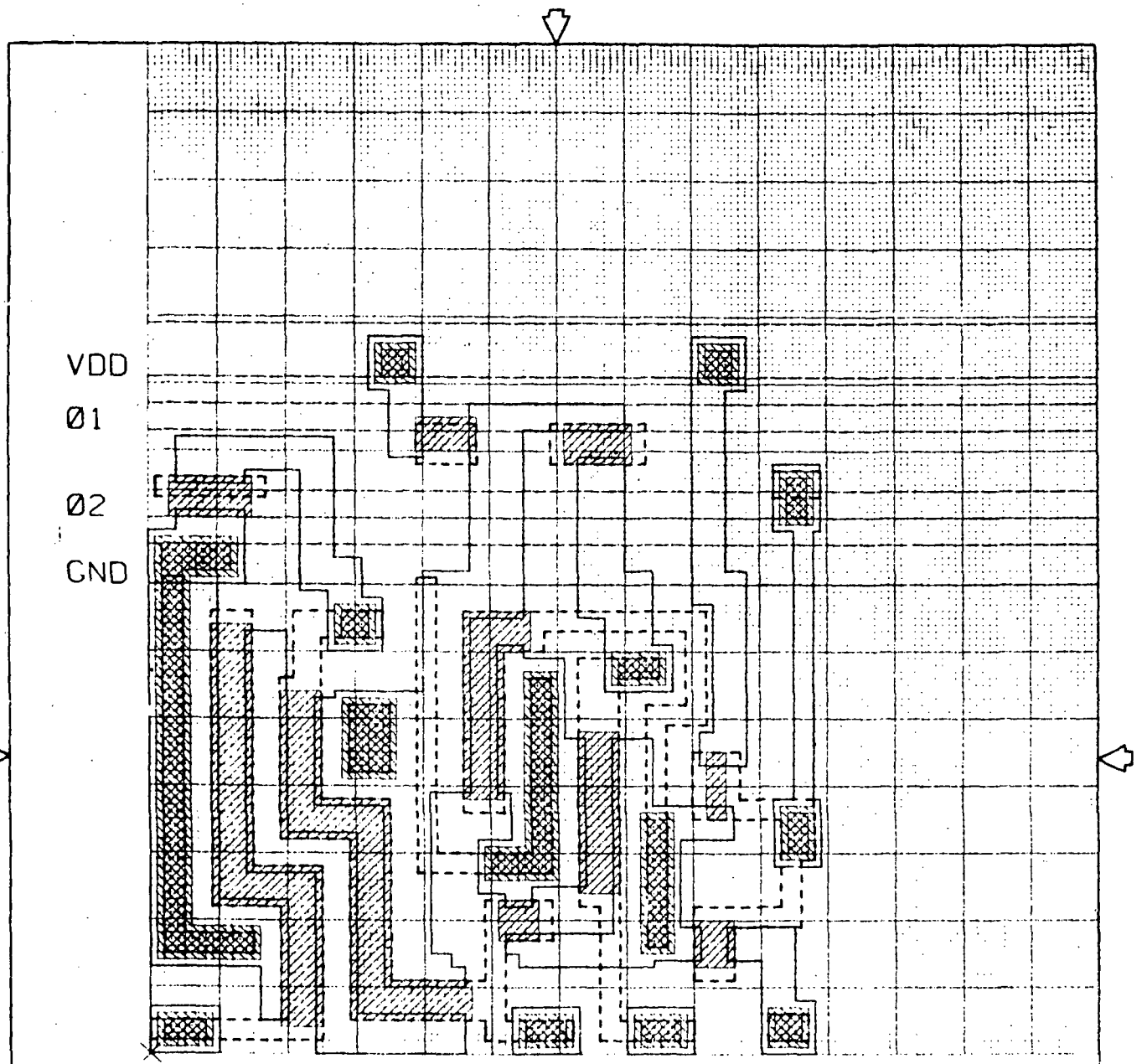
$$S \quad [\bar{B} \cdot \overline{P_{t-1}} + \bar{A} \cdot B]\, \phi_1 \cdot S_{t-1} \cdot \bar{\phi}_1$$

$$P \quad \overline{S_{t-1}} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$[\overline{B_{t-1}} \cdot P_{t-1} + A_{t-1} \cdot B_{t-1}]\, \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_B	3	1220
C_A	2	900
C_S	4	1110
C_P	5	640
PATTERN NO.		2660



2660

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		STATIC REGISTER Q, $\bar{Q}$ OUTPUT AND KILL
SCALE 0.1mil/div			SHEET

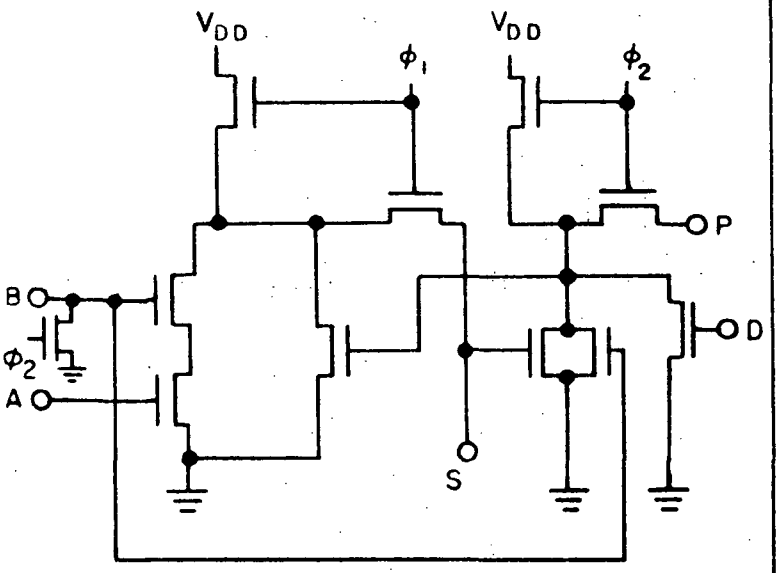
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 2pF
"0" AND "1" OUTPUTS, RESET AND KILL

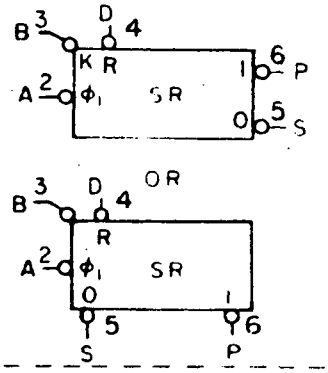
PATTERN NO. 2680 (ϕ_1, ϕ_2)

JUNE 1969

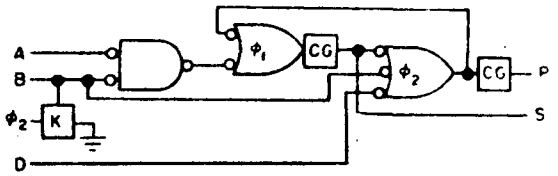
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	D	ϕ_1	S	ϕ_2	P
*	*	*	0	S_{t-1}	–	–
*	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
*	0	1	1	1	0	P_{t-1}
0	*	1	1	1	0	P_{t-1}
0	1	*	1	1	0	P_{t-1}
1	1	*	1	0	0	P_{t-1}
*	0	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	1	0	*	1	0
*	0	0	0	1	1	0
*	0	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT

LOGIC EQUATIONS

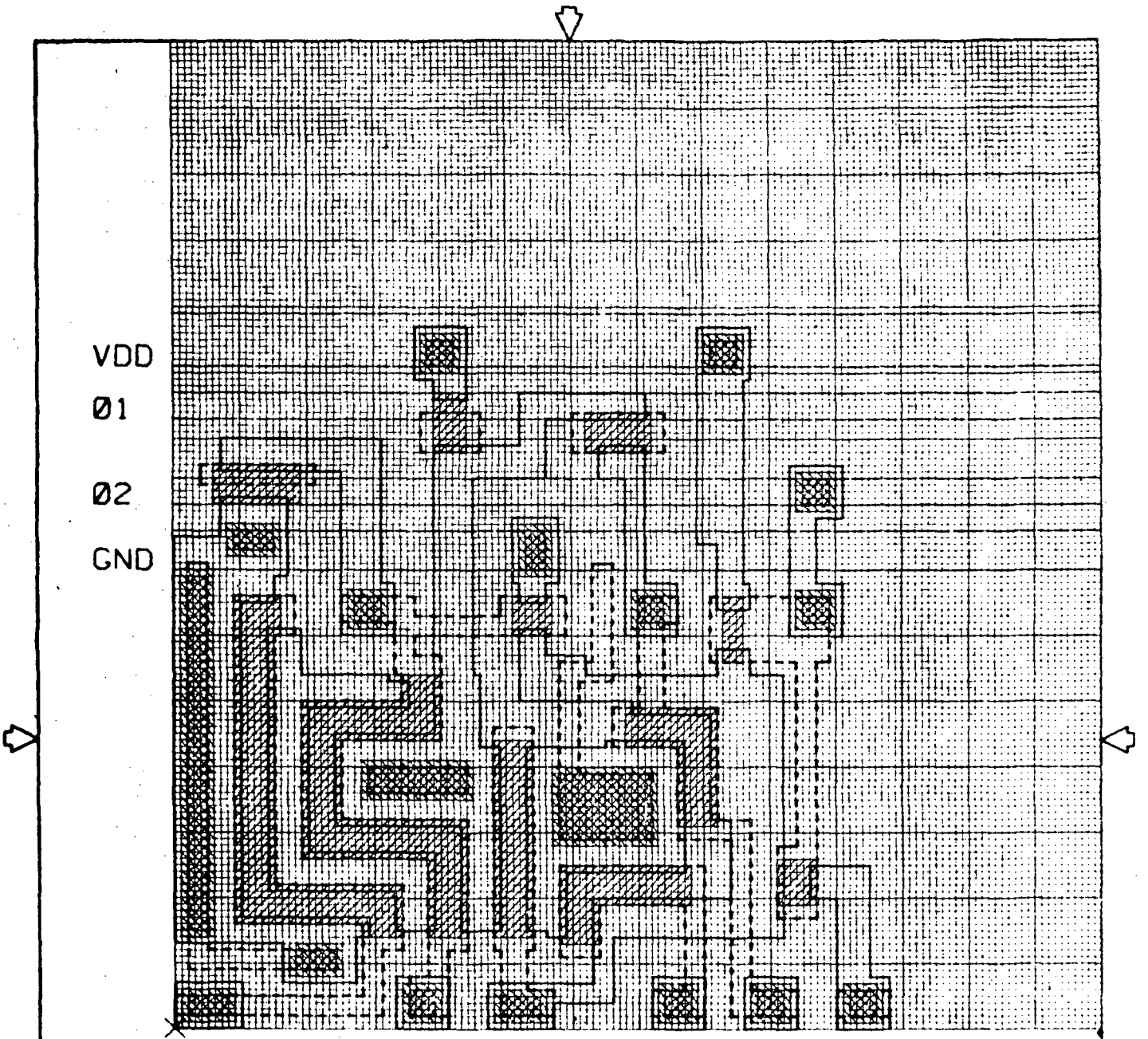
$$S = [(\bar{A} + \bar{B}) \cdot D + B \cdot \bar{A} + \bar{B} \cdot \bar{D} \cdot \overline{P_{t-1}}] \cdot \phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \overline{\phi_2}$$

$$= [A_{t-1} \cdot B_{t-1} \cdot \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	930
C_B	3	1240
C_S	5	950
C_P	6	840
C_D	4	370
PATTERN NO.		2680



2680

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		**STATIC REGISTER Q, $\bar{Q}$ OUTPUT W/RESET AND KILL**
SCALE 0.1mil/div			SHEET

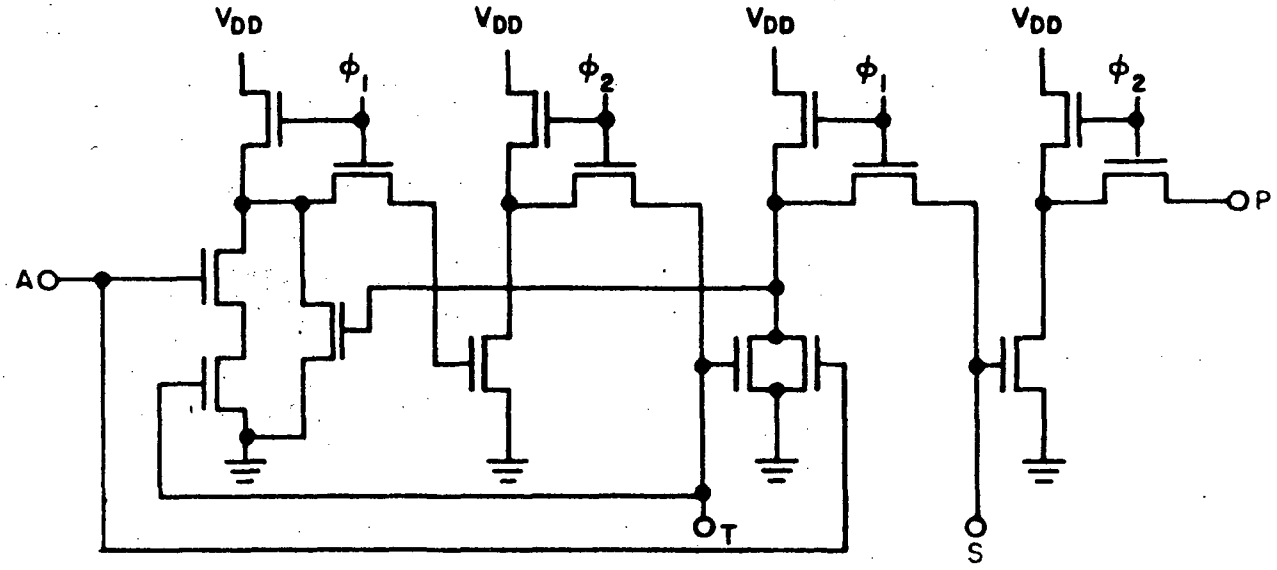
BANNING THICK OXIDE STANDARD CELL

BINARY, 2pF
"0", CARRY AND CARRY NOT OUTPUTS

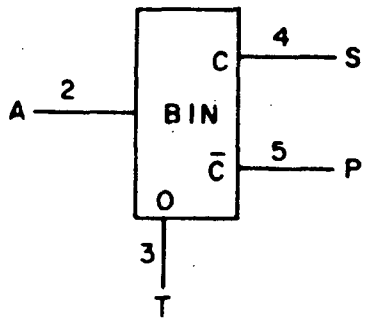
PATTERN NO. 2700 (ϕ_2)

APRIL 1968

SCHEMATIC

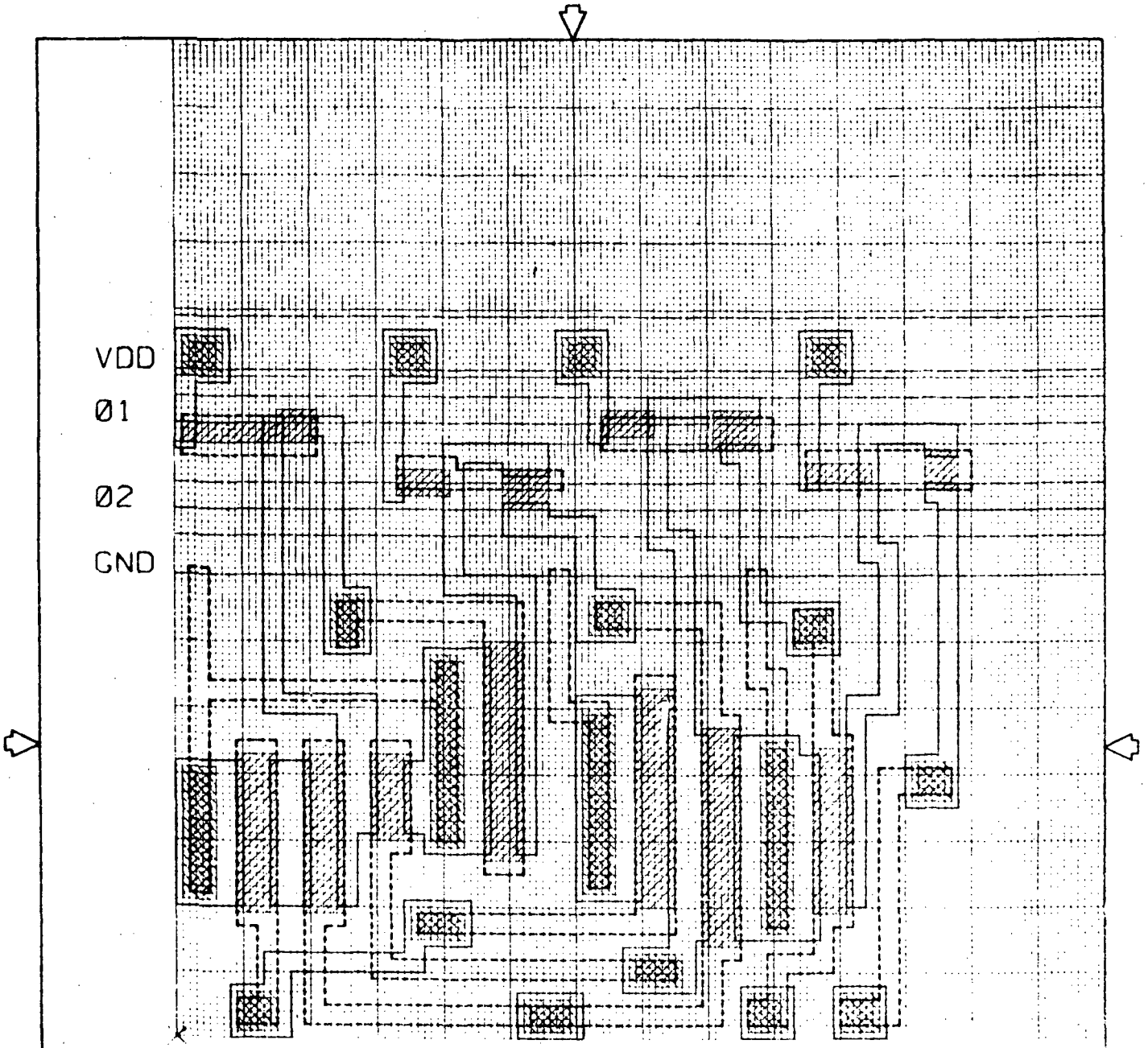


LOGIC SYMBOL



CELL I/O CAPACITIES		
CAPACITOR	**PIN**	**CAPACITY IN fF**
C_A	2	880
C_T	3	1060
C_S	4	880
C_P	5	360
PATTERN NO.		2700

NOTE: THIS CELL HAS SEVERAL MODES OF OPERATION. SEE SECTION 4E7.



2700

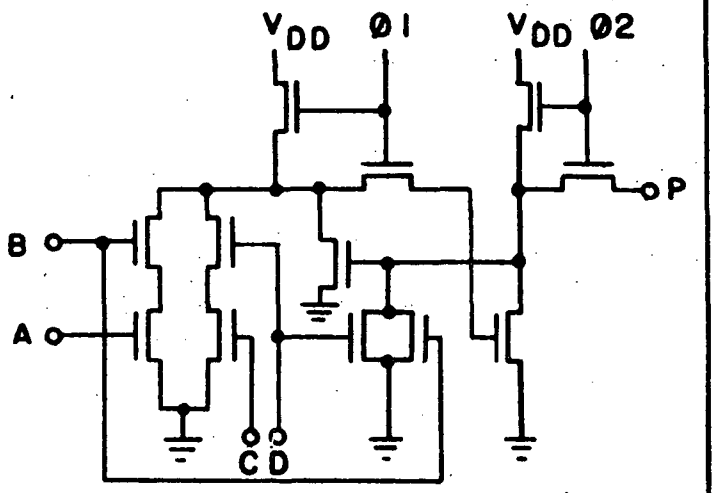
SIZE	CODE IDENT. NO.	DWG. NO.	
A	98230		**BINARY $\overline{Q}$, CARRY, $\overline{\text{CARRY}}$ OUTPUT**
SCALE **0.1 mil/div**			SHEET

BANNING THICK OXIDE STANDARD CELL

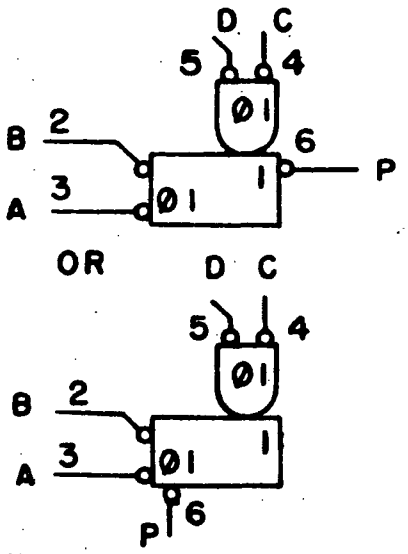
DUAL SAMPLE REGISTER, 2_pF PATTERN NO. 2720($\emptyset_1\emptyset_2$)
"1" OUTPUT

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE					
J_{t-1}	K_{t-1}	$\emptyset_1$	J	$\emptyset_2$	P
*	*	*	*	0	P_{t-1}
0	*	0	0	1	P_{t-1}
1	0	0	0	1	0
1	1	0	0	1	1

* MEANS EITHER STATE

J=B+D LOGIC EQUATIONS K=A·B+C·D

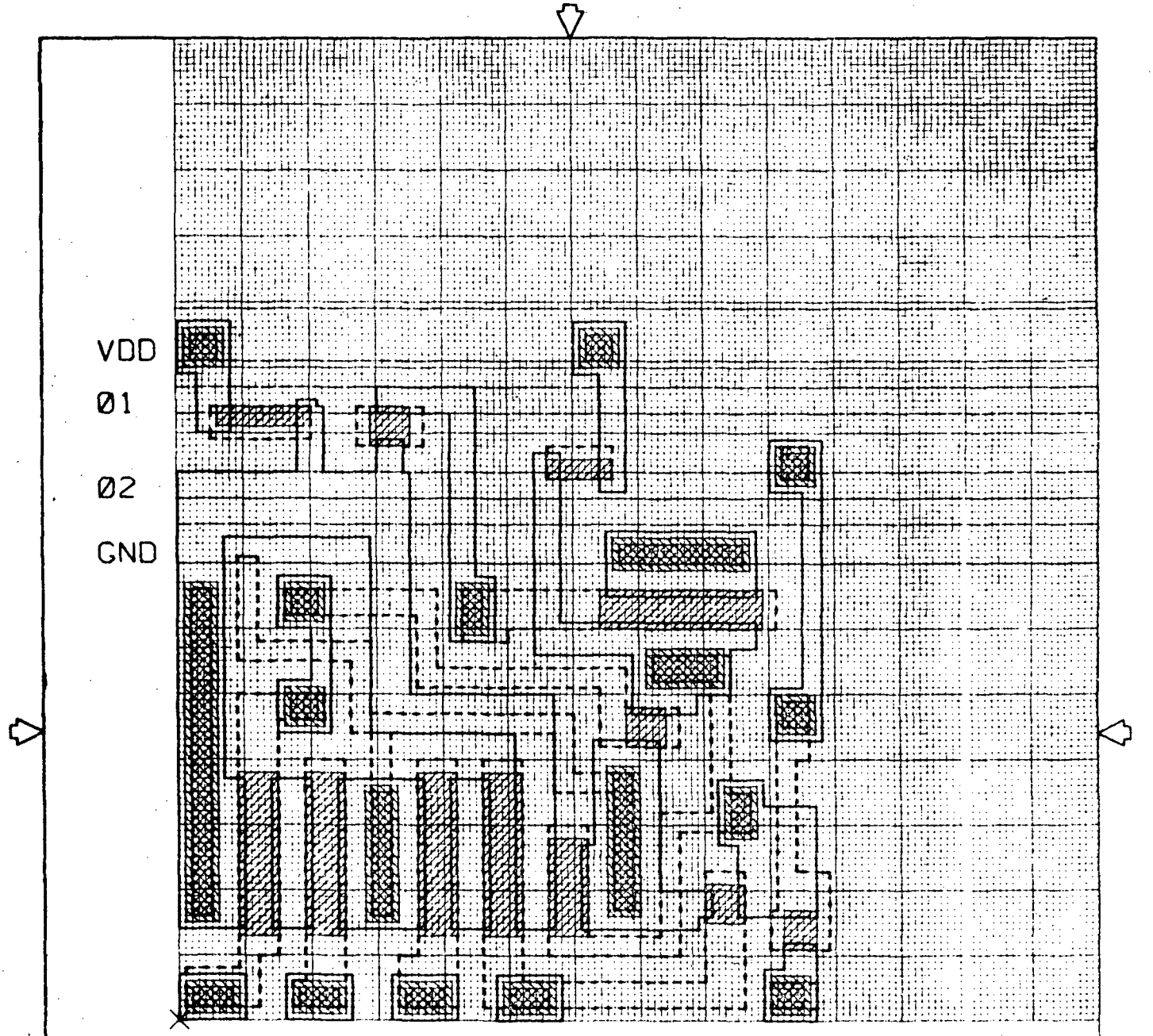
$$P = (K_{t-1} + \overline{J_{t-1}} \cdot \overline{K_{t-1}} \cdot P_{t-1}) \cdot \overline{D} \cdot \overline{B} \cdot \emptyset_2 + P_{t-1} \cdot \overline{\emptyset_2}$$

CELL I/O CAPACITIES		
CAPACITOR	PIN	CAPACITY IN fF
C_B	2	600
C_A	3	360
C_C	4	360
C_D	5	470
C_P	6	560
PATTERN NO.		2720

B AND D ARE SAMPLE INPUTS
DURING $\emptyset_2$ B AND D MUST
EQUAL ZERO

DS-60A

DUAL SAMPLE REGISTER · 2720 · JUNE 1969
"1" OUTPUT



2720

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		DUAL SAMPLE REGISTER Q OUT
SCALE 0.1mil/div			SHEET

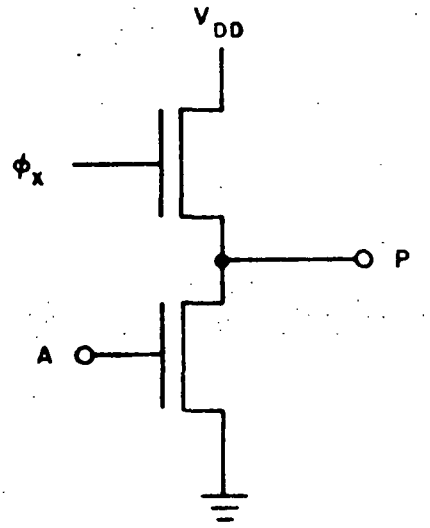
BANNING THICK OXIDE STANDARD CELL

INVERTER, 4pF

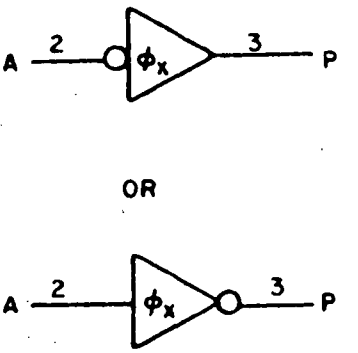
PATTERN NO. 4010 [ϕ_1]
4020 [ϕ_2]

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_x	P
0	0	P_{t-1}
1	*	0
0	1	1

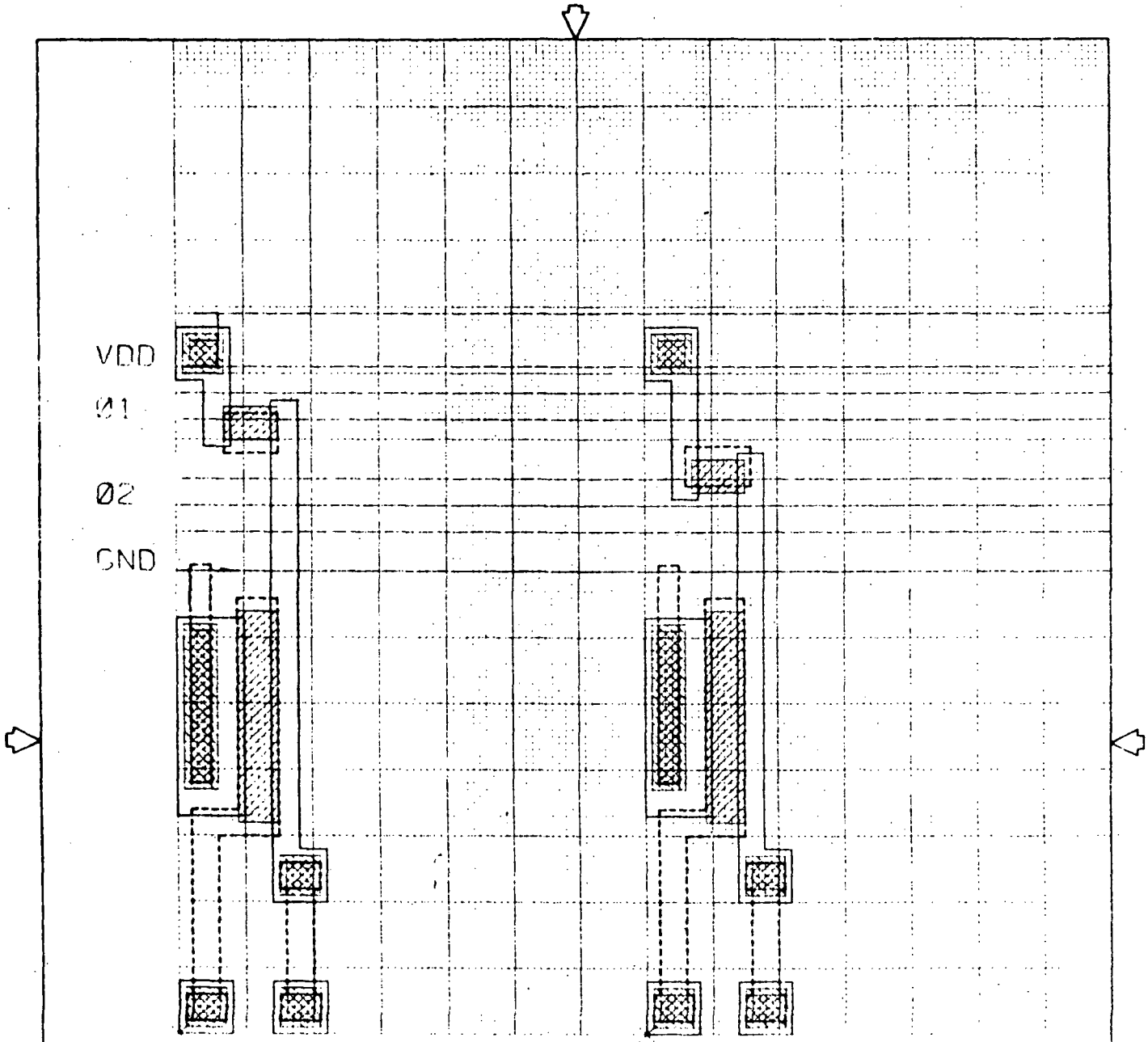
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{A} \cdot \bar{\phi}_x + \bar{A} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	460	460
C_P	3	280	270
PATTERN NO.		4010	4020



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		**INVERTER**
SCALE **0.1mil/div**			SHEET

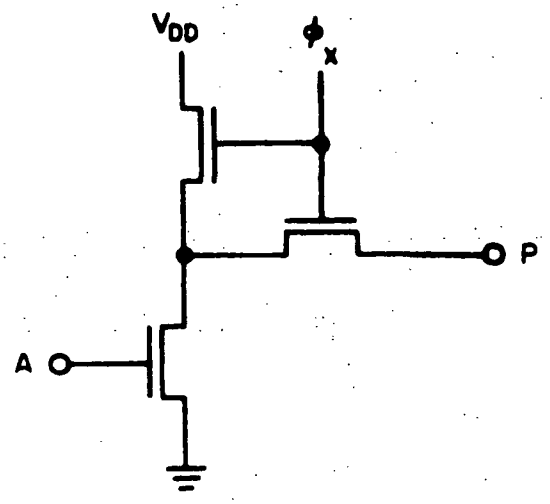
BANNING THICK OXIDE STANDARD CELL

INVERTER WITH DELAY, 4pF

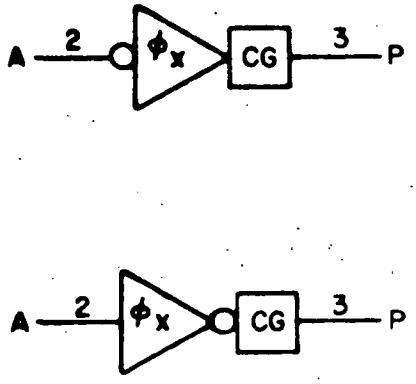
PATTERN NO. 4050 (ϕ_1) / 4060 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_x	P
*	0	P_{t-1}
1	1	0
0	1	1

*MEANS EITHER STATE

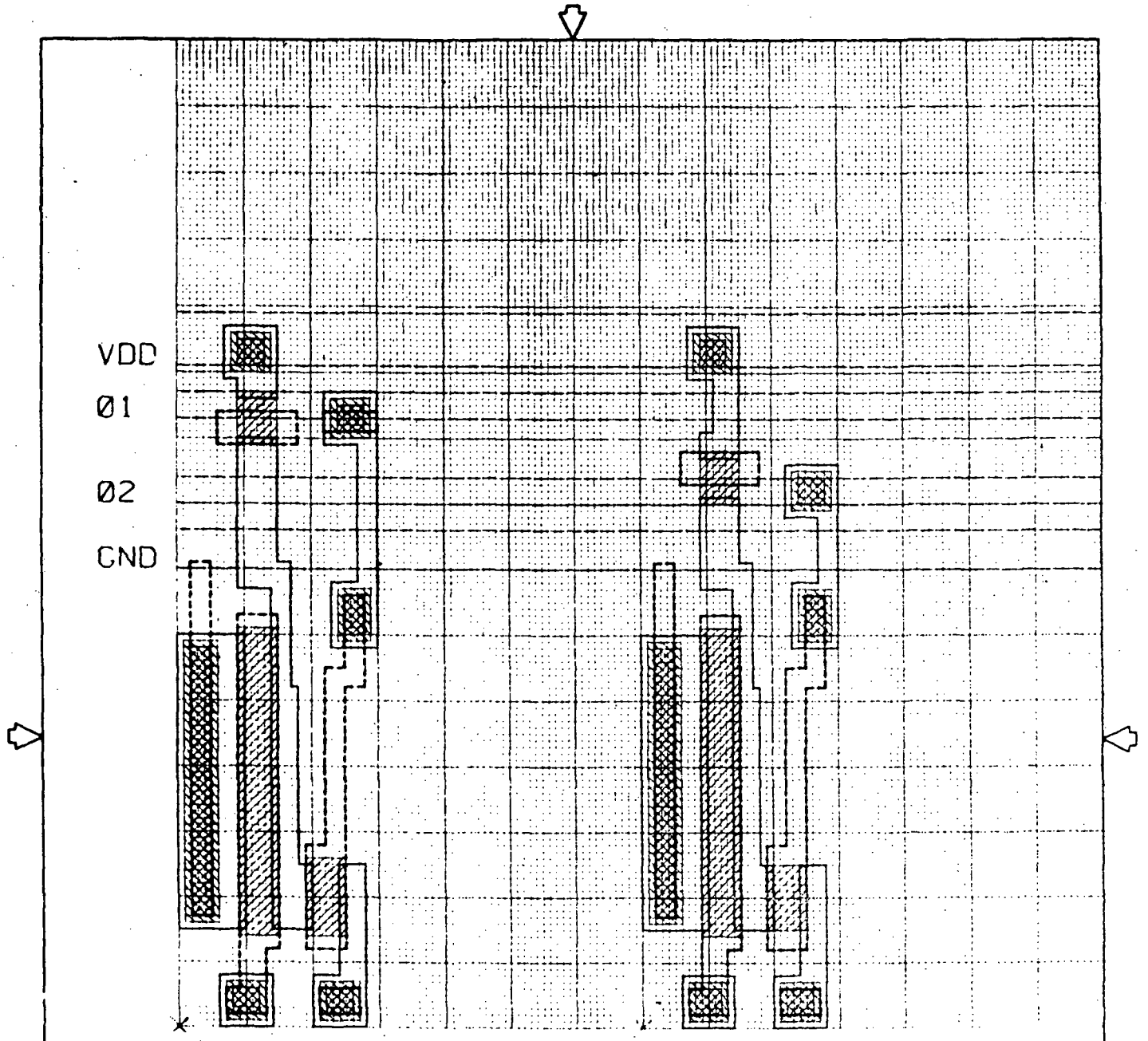
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{\phi}_x + \bar{A} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	620	620
C_P	3	280	250
PATTERN NO.		4050	4060

INVERTER WITH DELAY • 4050 4060 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		INVERTER W/DELAY
SCALE 0.1mil/div			SHEET

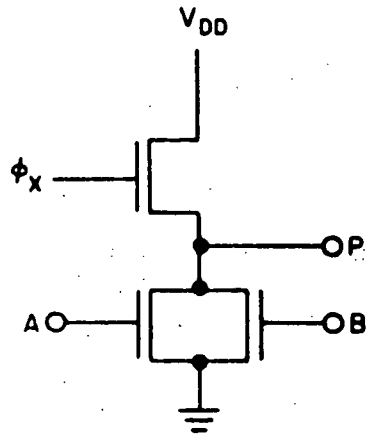
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NOR, 4pF

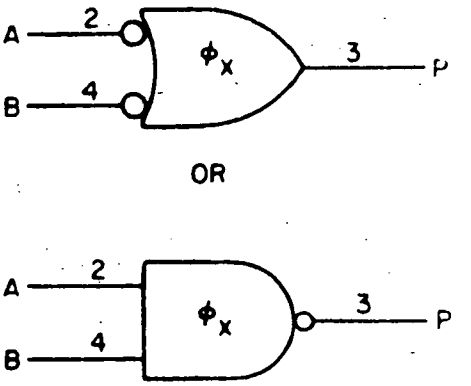
PATTERN NO. 4070 (ϕ_1)
4080 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_X	P
0	0	0	P_{t-1}
1	*	*	0
*	1	*	0
0	0	1	1

*MEANS EITHER STATE

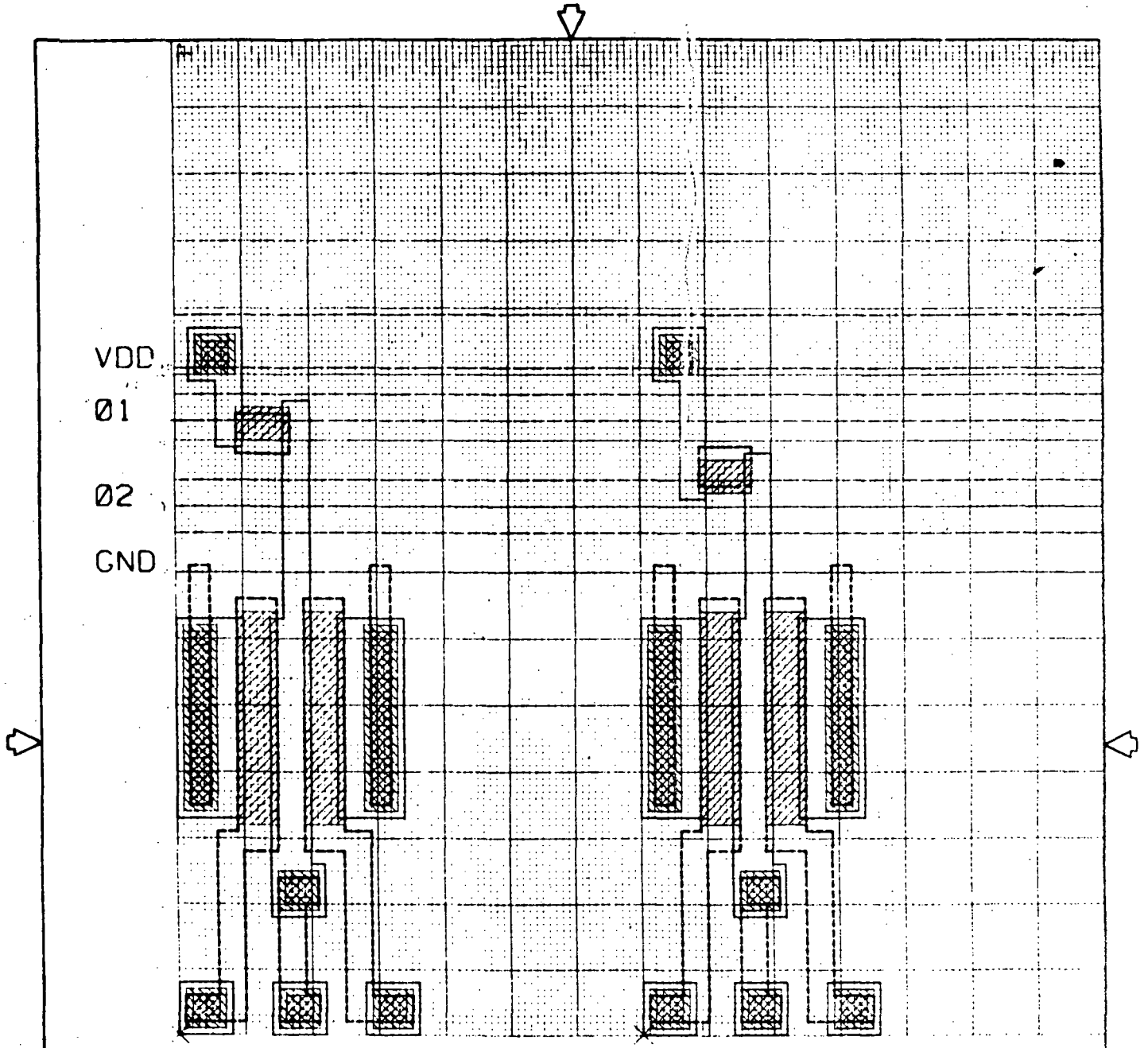
LOGIC EQUATIONS

$$P = (\overline{A + B}) \cdot \bar{\phi}_X \cdot P_{t-1} + (\overline{A + B}) \cdot \phi_X$$

$$= \bar{A} \cdot \bar{B} \cdot \bar{\phi}_X \cdot P_{t-1} + \bar{A} \cdot \bar{B} \cdot \phi_X$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	460	460
C_P	3	350	330
C_B	4	460	460
PATTERN NO.		4070	4080



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NOR
SCALE 0.1mil/div		SHEET

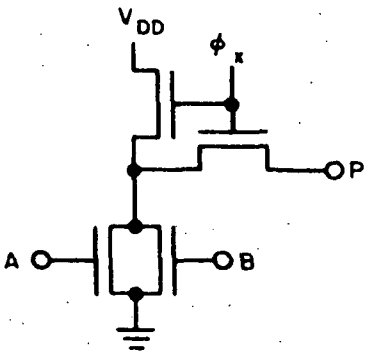
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NOR WITH DELAY, 4pF

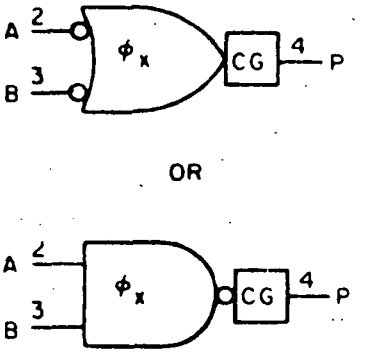
PATTERN NO. 4090 (ϕ_1)
4100 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
*	*	0	P_{t-1}
1	*	1	0
*	1	1	0
0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi}_x + \overline{(A + B)} \cdot \phi_x$$

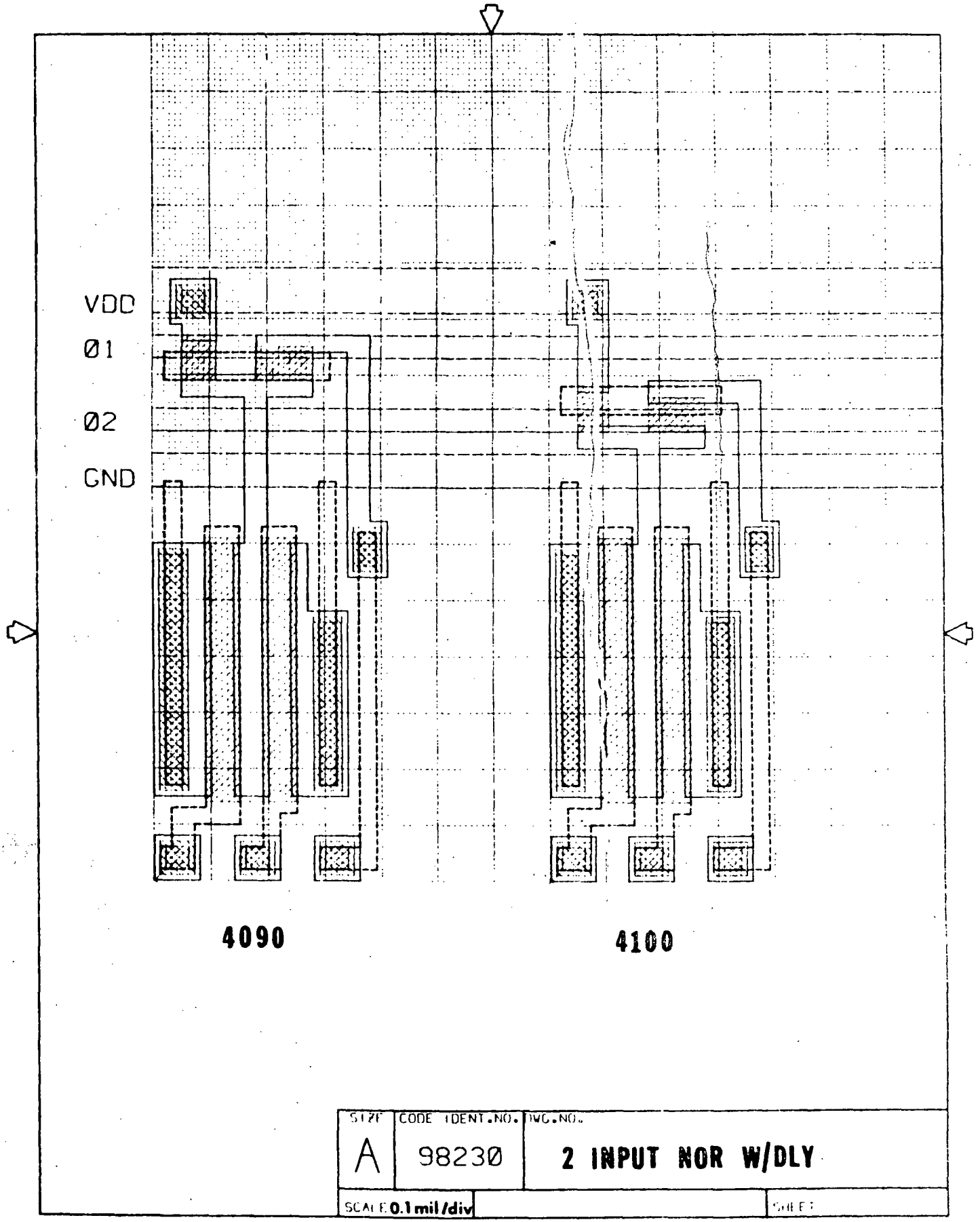
$$= (P_{t-1}) \cdot \overline{\phi}_x + \overline{A} \cdot \overline{B} \cdot \phi_x$$

PATTERN NO.

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	620	620
C_B	3	620	620
C_P	4	500	470
PATTERN NO.		4090	4100

TWO INPUT NOR WITH DELAY • 4090 4100 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NOR W/DLY
SCALE 0.1 mil/div		SHEET

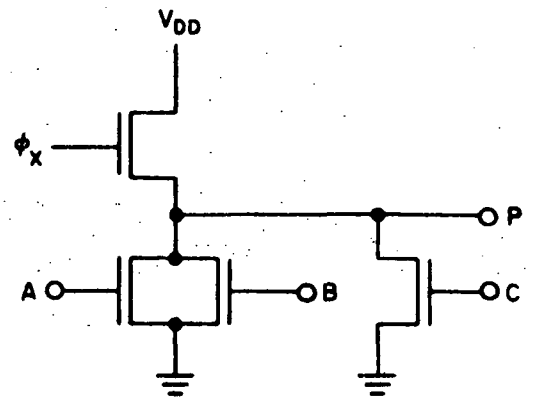
BANNING THICK OXIDE STANDARD CELL

THREE INPUT NOR, 4pF

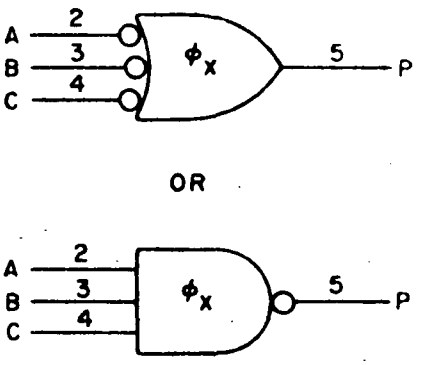
PATTERN NO. 4110 (ϕ_1)
4120 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_X	P
0	0	0	0	P_{t-1}
1	*	*	*	0
*	1	*	*	0
*	*	1	*	0
0	0	0	1	1

*MEANS EITHER STATE

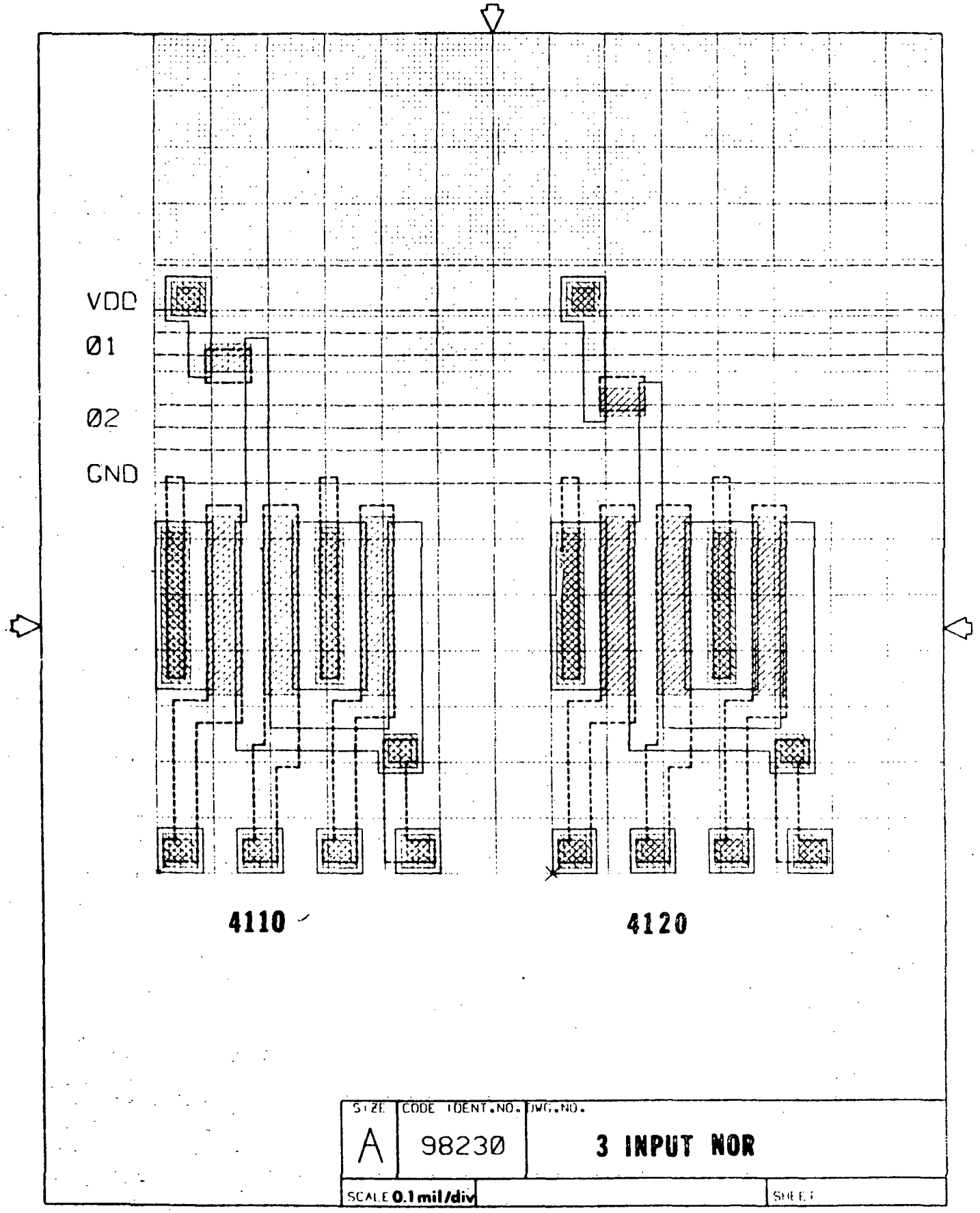
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi_X} \cdot \overline{(A + B + C)} + \overline{(A + B + C)} \cdot \phi_X$$

$$= (P_{t-1}) \cdot \overline{\phi_X} \cdot \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \phi_X$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	460	460
C_B	3	460	460
C_C	4	460	460
C_P	5	580	550
PATTERN NO.		4110	4120



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	3 INPUT NOR
SCALE 0.1 mil/div		SHEET

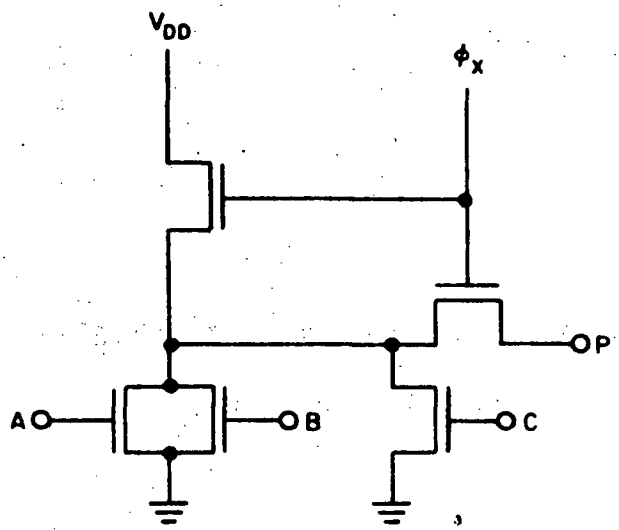
BANNING THICK OXIDE STANDARD CELL

THREE INPUT NOR WITH DELAY, 4pF

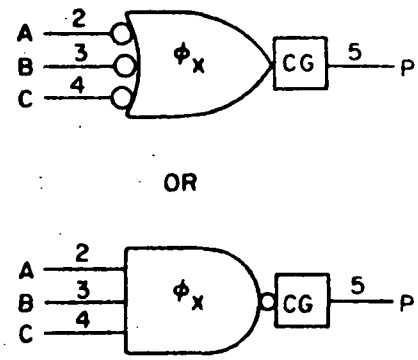
PATTERN NO. 4130 (ϕ_1)
4140 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_X	P
*	*	*	0	P_{t-1}
1	*	*	1	0
*	1	*	1	0
*	*	1	1	0
0	0	0	1	1

*MEANS EITHER STATE

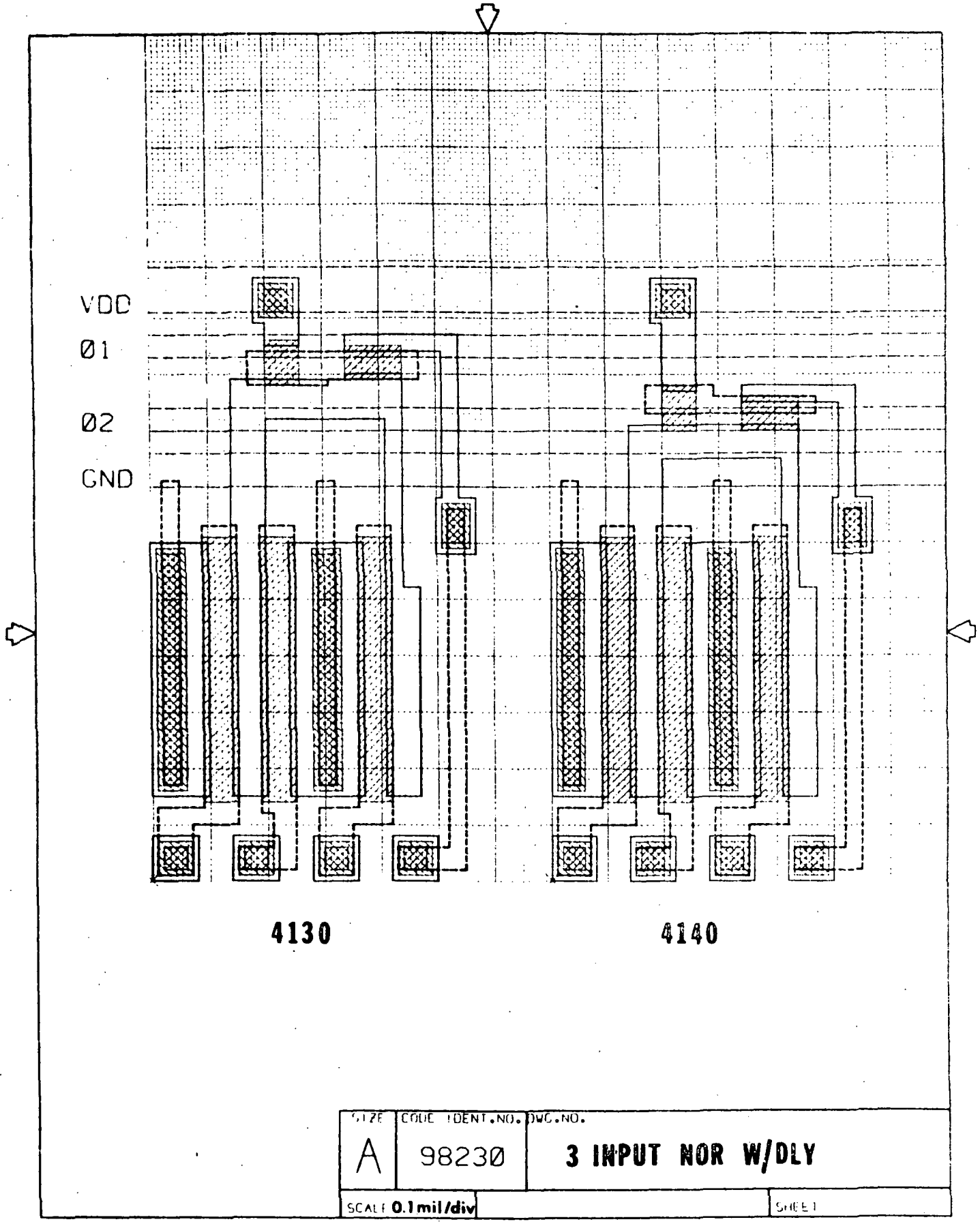
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi}_X + \overline{(A + B + C)} \cdot \phi_X$$

$$= (P_{t-1}) \cdot \overline{\phi}_X + \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \phi_X$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	620	620
C_B	3	620	620
C_C	4	620	620
C_P	5	720	650
PATTERN NO.		4130	4140



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		3 INPUT NOR W/DLY
SCALE 0.1 mil/div			SHEET

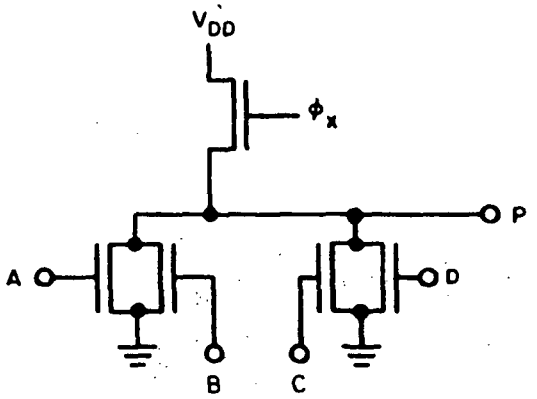
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT NOR, 4pF

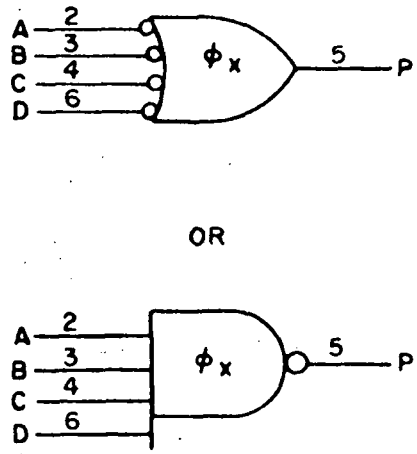
PATTERN NO. 4150 (ϕ_1)
4160 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	ϕ_x	P
0	0	0	0	0	P_{t-1}
1	*	*	*	*	0
*	1	*	*	*	0
*	*	1	*	*	0
*	*	*	1	*	0
0	0	0	0	1	1

*MEANS EITHER STATE

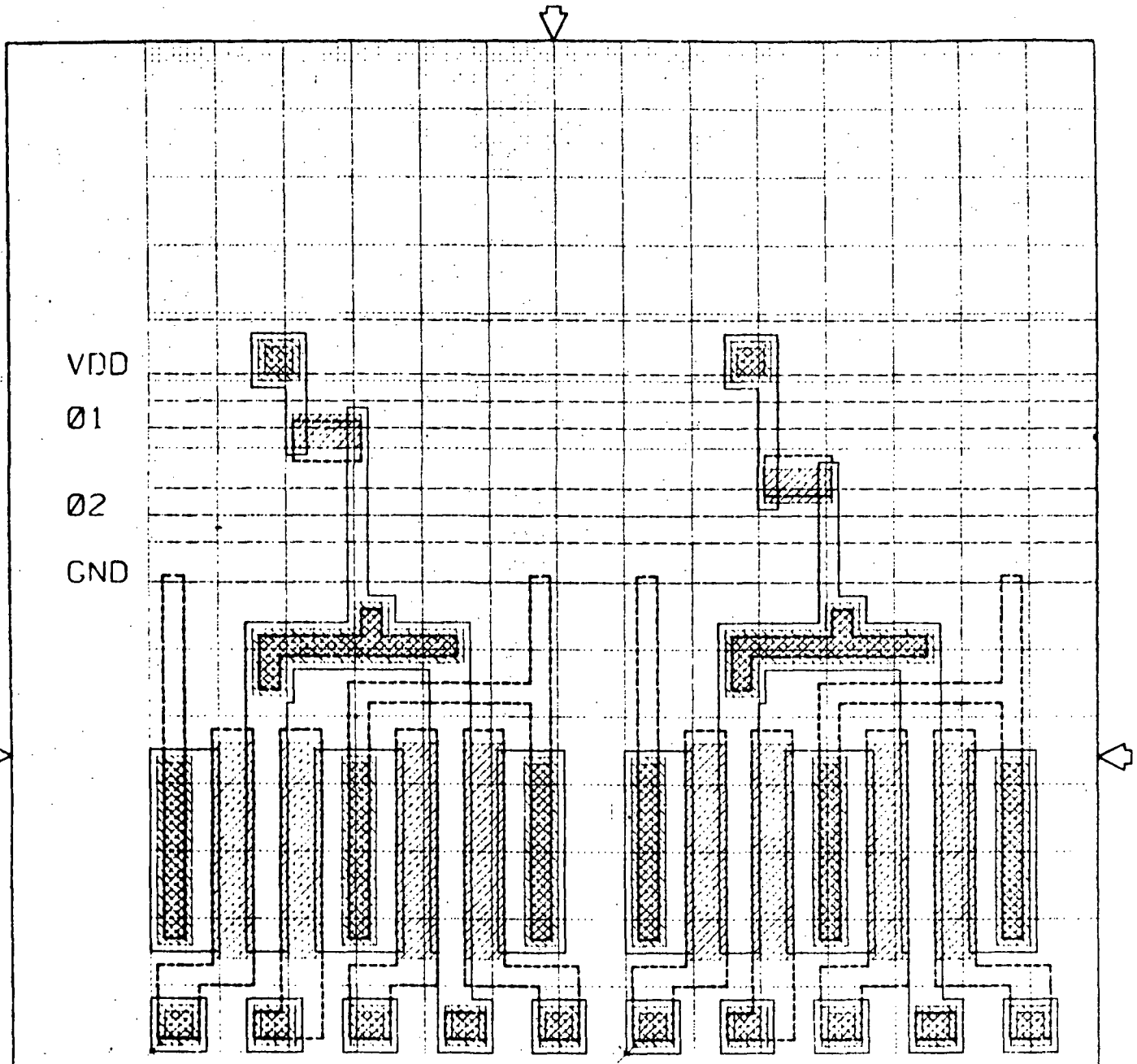
LOGIC EQUATIONS

$$P = P_{t-1} \cdot \overline{(A + B + C + D)} \cdot \bar{\phi}_x + \overline{(A + B + C + D)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{\phi}_x + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	440	440
C_B	3	440	440
C_C	4	440	440
C_P	5	670	650
C_D	6	440	440
PATTERN NO.		4150	4160



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	4 INPUT NOR
SCALE 0.1 mil/div		SHEET

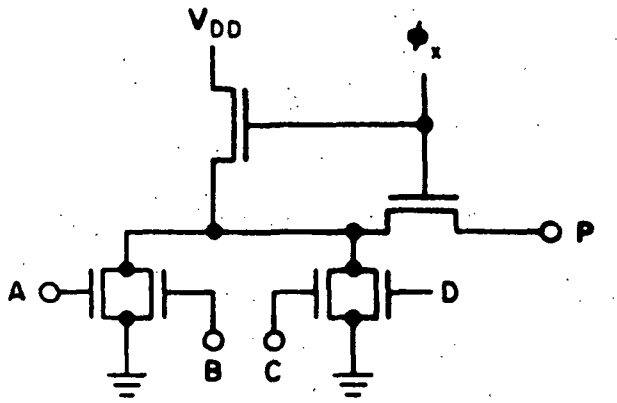
BANNING THICK OXIDE STANDARD CELL

FOUR INPUT NOR WITH DELAY, 4pF

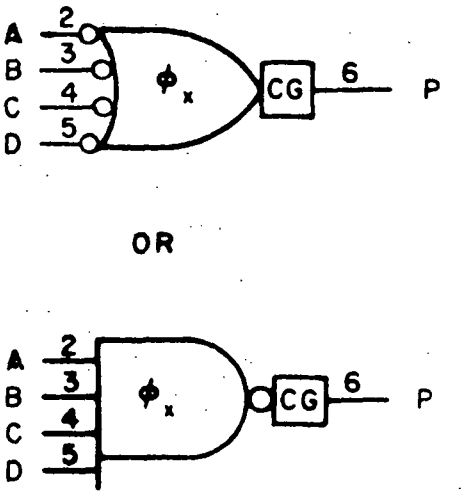
PATTERN NO.4170 (ϕ_1)
4180 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

(A + B + C + D)	ϕ_x	P
*	0	P_{t-1}
1	1	0
0	1	1

*MEANS EITHER STATE

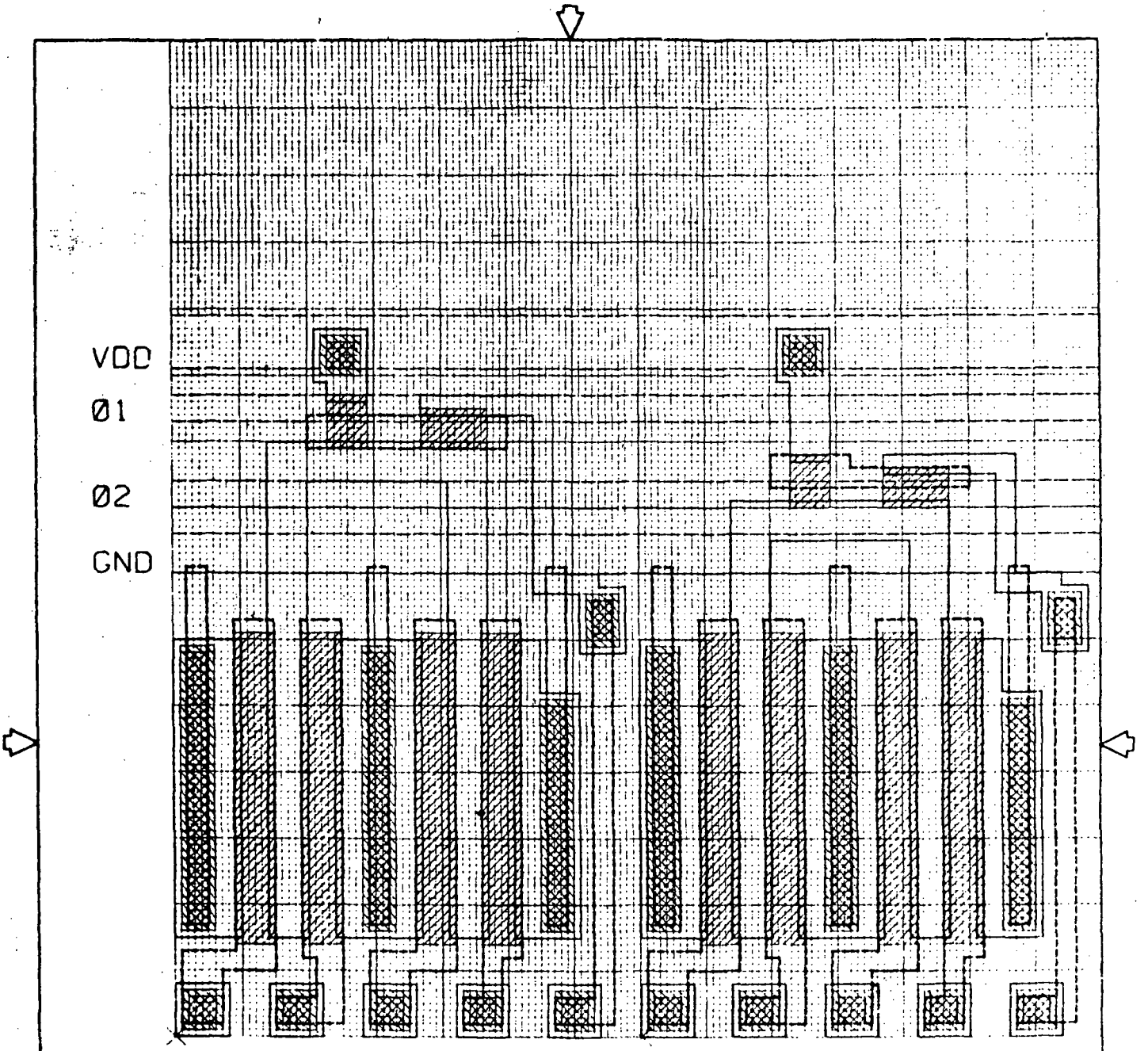
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{\phi}_x + \overline{(A + B + C + D)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot \bar{\phi}_x + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	620	620
C_B	3	620	620
C_C	4	620	620
C_D	5	620	620
C_P	6	780	720
PATTERN NO.		4170	4180



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	4 INPUT NOR W/DLY	
SCALE 0.1mil/div			SHEET

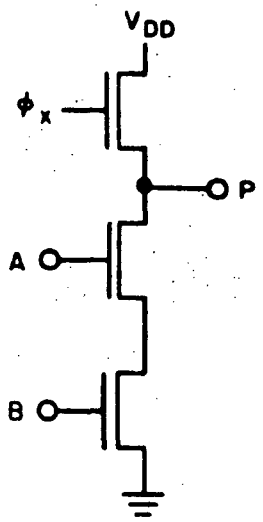
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NAND, 4pF

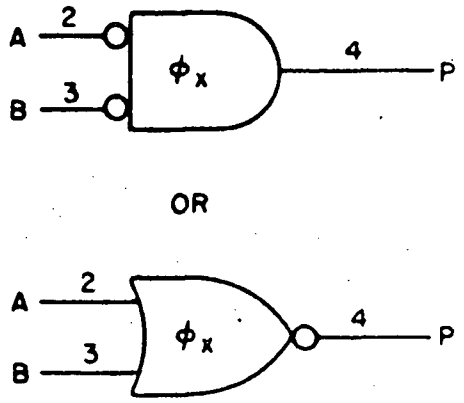
PATTERN NO. 4190 (ϕ_1)
4200 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
0	*	0	P_{t-1}
*	0	0	P_{t-1}
1	1	*	0
0	*	1	1
*	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

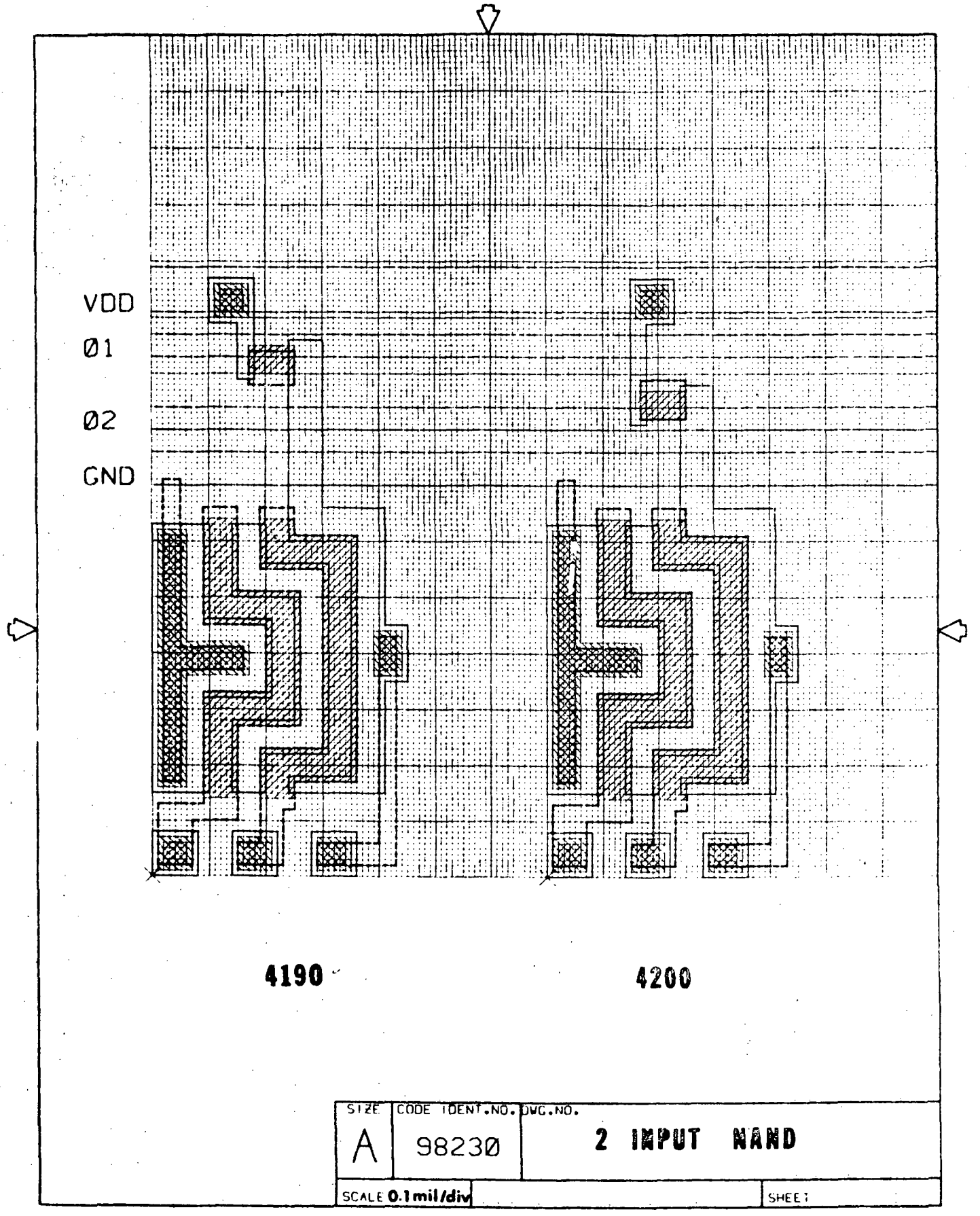
$$P = (P_{t-1}) \cdot \overline{(A \cdot B)} \cdot \overline{\phi}_x + \overline{(A \cdot B)} \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\overline{A} + \overline{B}) \cdot \overline{\phi}_x + (\overline{A} + \overline{B}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	920	920
C_B	3	920	920
C_P	4	510	470
PATTERN NO.		4190	4200

TWO INPUT NAND • 4190 4200 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		2 INPUT NAND
SCALE 0.1mil/div			SHEET

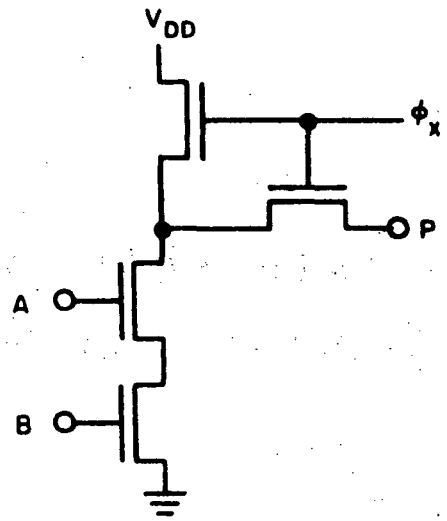
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NAND WITH DELAY, 4pF

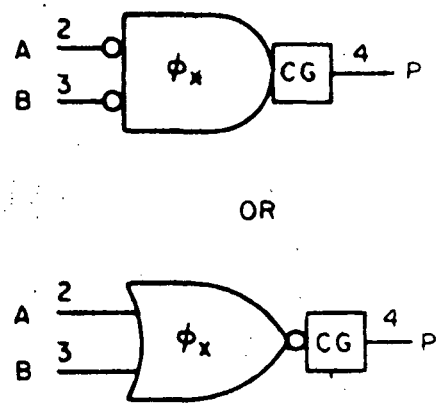
PATTERN NO. 4210 [ϕ_1]
4220 [ϕ_2]

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
*	*	0	P_{t-1}
1	1	1	0
0	*	1	1
*	0	1	1

*MEANS EITHER STATE

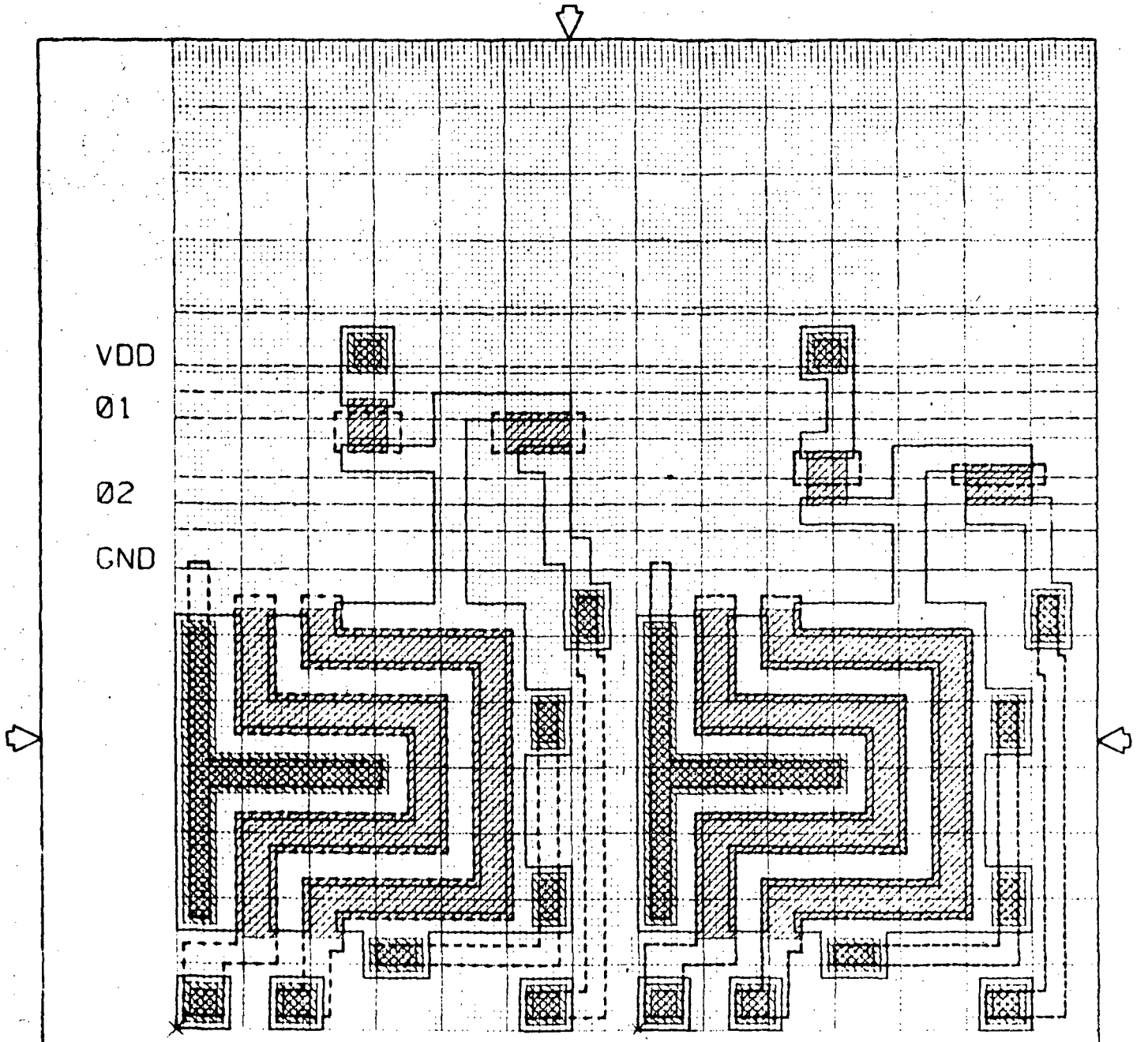
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi}_x + (\overline{A \cdot B}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot \overline{\phi}_x + (\overline{A} + \overline{B}) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	1280	1280
C_B	3	1280	1280
C_P	4	660	640
PATTERN NO.		4210	4220



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NAND W/DLY
SCALE 0.1mil/div		SHEET

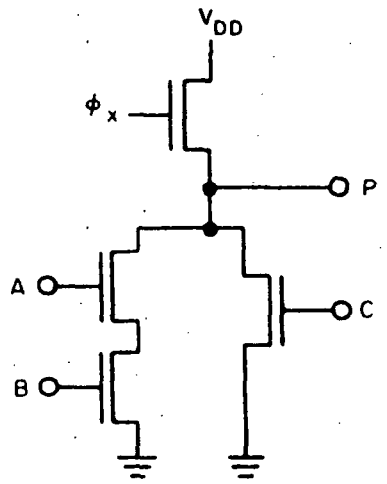
BANNING THICK OXIDE STANDARD CELL

THREE INPUT AND NOR, 4pF

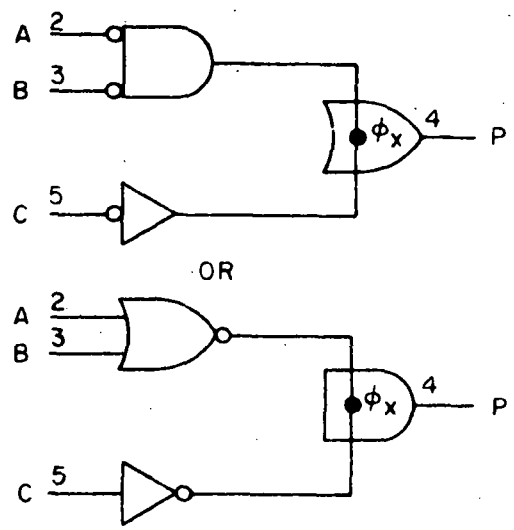
PATTERN NO. 4230 (ϕ_1)
4240 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
0	*	0	0	P_{t-1}
*	0	0	0	P_{t-1}
*	*	1	*	0
1	1	*	*	0
0	*	0	1	1
*	0	0	1	1

*MEANS EITHER STATE

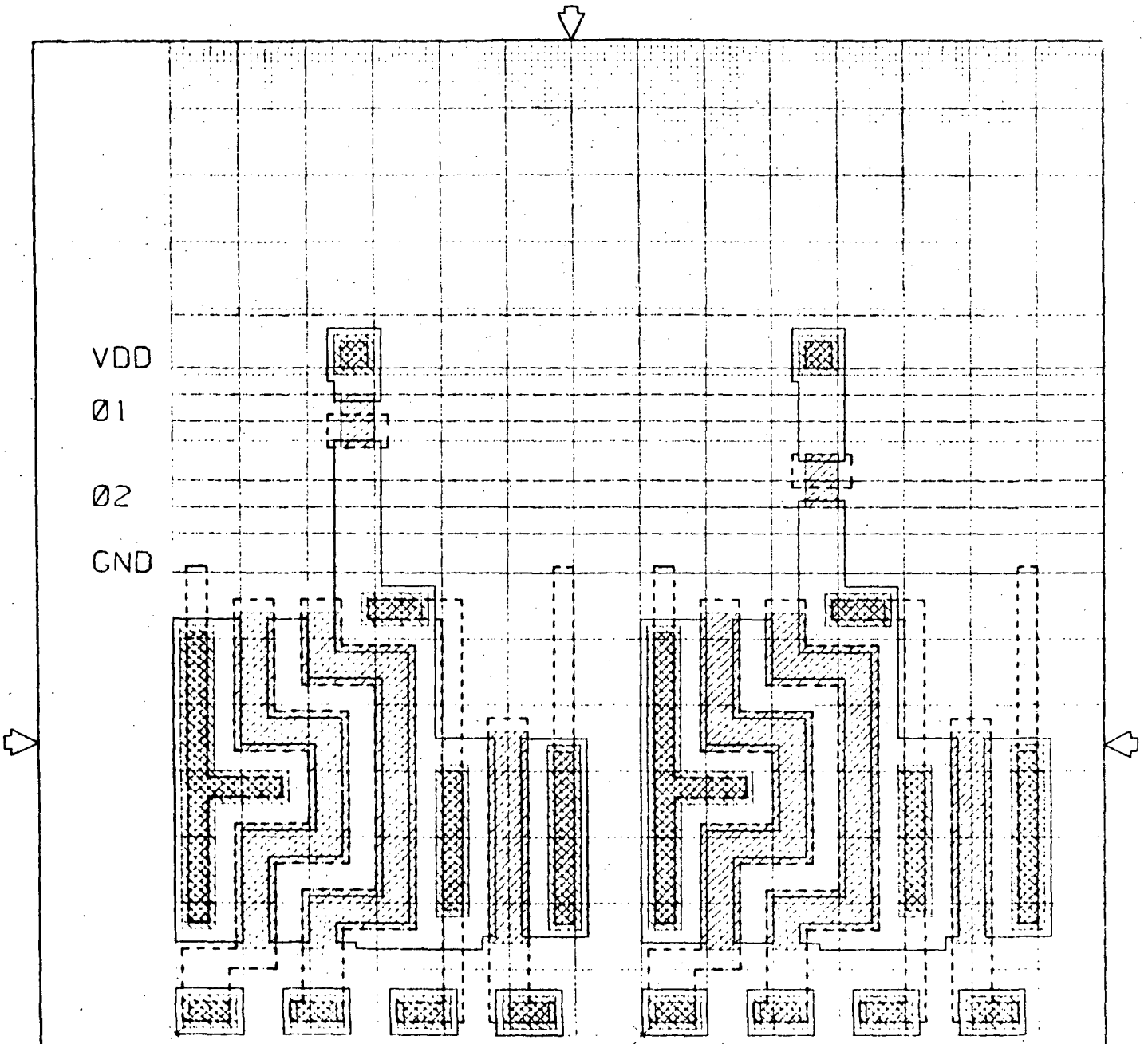
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{(A \cdot B + C)} \cdot \overline{\phi}_x + \overline{(A \cdot B + C)} \cdot \phi_x$$

$$(P_{t-1}) \cdot (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \overline{\phi}_x + (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \phi_x$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	940	940
C_B	3	940	940
C_C	4	640	600
C_D	5	450	450
PATTERN NO.		4230	4240



SIZE	CODE IDENT.NO.	DRAWING NO.
A	98230	3 INPUT AND NOR 4PF
SCALE 0.1mil/div		SHEET

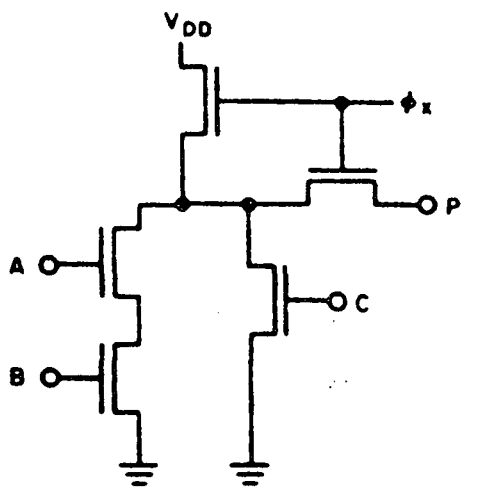
BANNING THICK OXIDE STANDARD CELL

THREE INPUT AND NOR WITH DELAY, 4pF

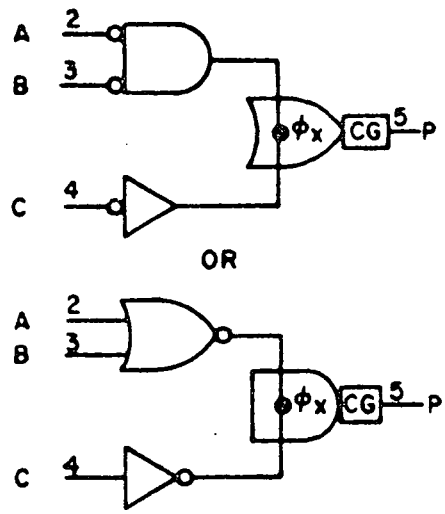
PATTERN NO. 4250 (ϕ_1)
4260 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
•	•	•	0	P_{t-1}
•	•	1	1	0
1	1	•	1	0
0	•	0	1	1
•	0	0	1	1

•MEANS EITHER STATE

LOGIC EQUATIONS

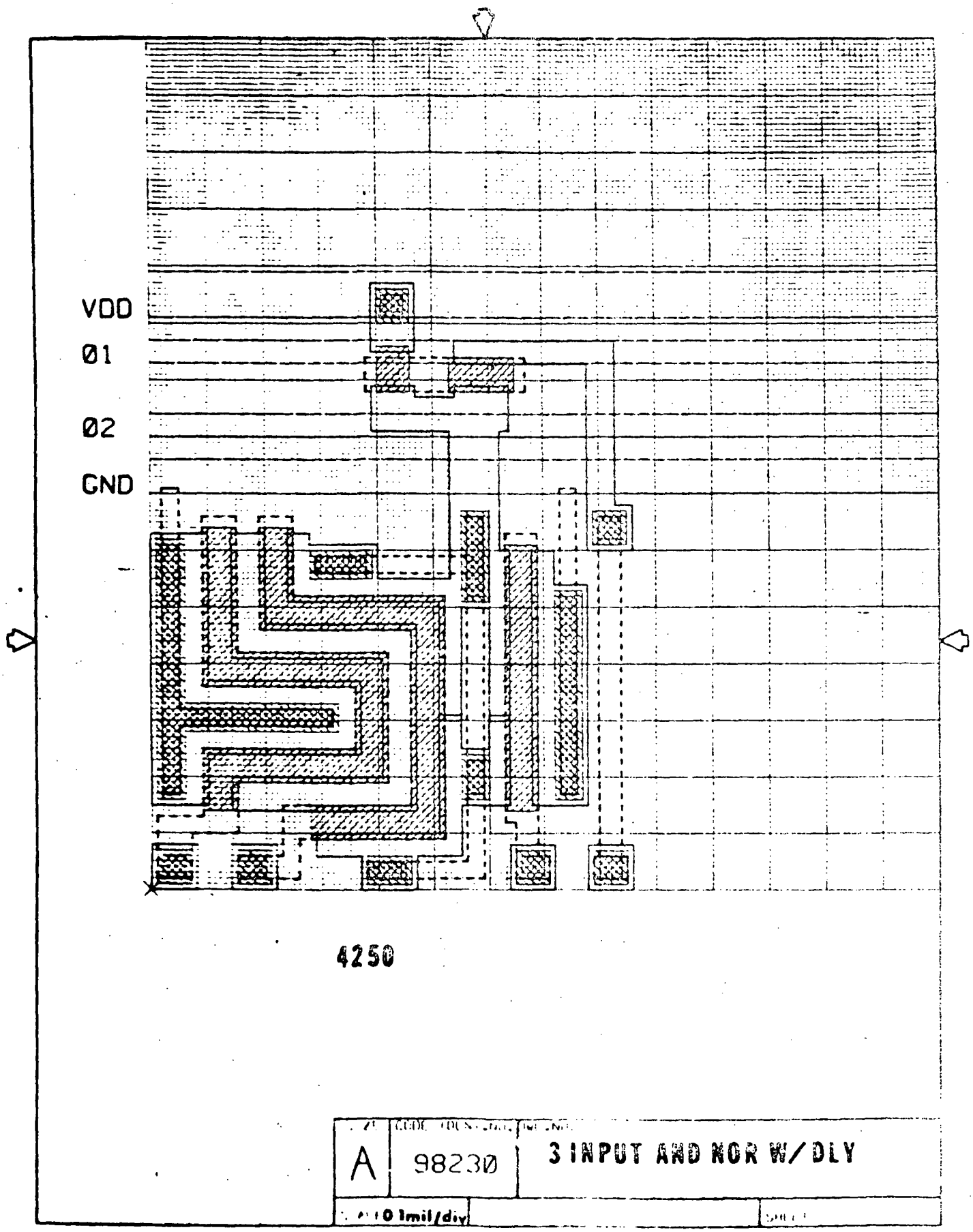
$$P = (P_{t-1}) \cdot \overline{\phi_x} + (\overline{A \cdot B + C}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot \overline{\phi}_x + (\bar{A} + \bar{B}) \cdot \bar{C} \cdot \phi_x$$

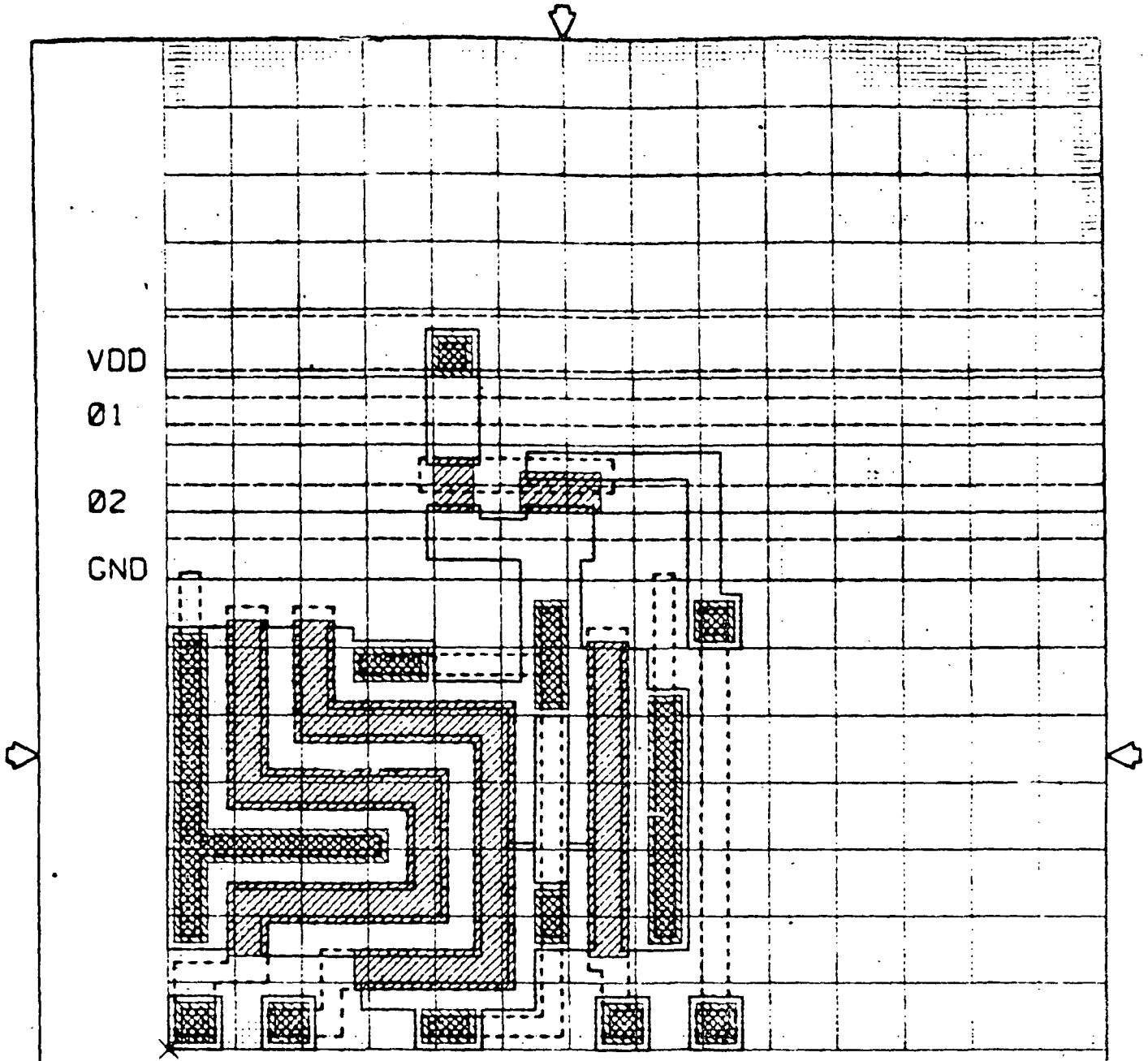
CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	1310	1310
C_B	3	1260	1260
C_C	4	620	620
C_P	5	970	910
PATTERN NO.		4250	4260

THREE INPUT AND NOR WITH DELAY • 4250 4260 • APRIL 1968



A	98230	3 INPUT AND NOR W/ DLY
0.1mil/div		



4260

SIZE	CODE IDENT. NO. (DRAWING)	3 INPUT AND NOR W/ DLY
A	98230	
SCALE 0.1mil/div		SHEET

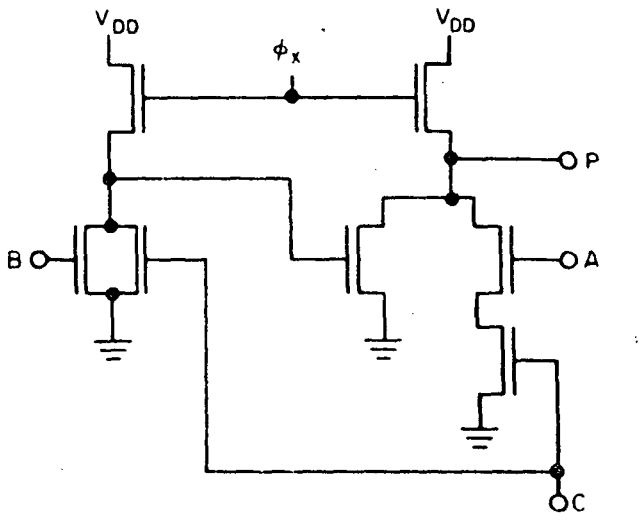
BANNING THICK OXIDE STANDARD CELL

THREE INPUT SWITCH, 4pF
(OPTIONAL EXCLUSIVE OR)

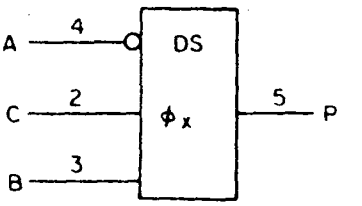
PATTERN NO. 4350 (ϕ_1)
4360 (ϕ_2)

APRIL 1968

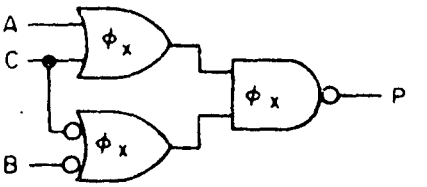
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	C	ϕ_x	P
*	*	0	0	P_{t-1}
0	*	*	0	P_{t-1}
1	*	1	*	0
*	0	0	1	0
*	1	0	1	1
0	*	1	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

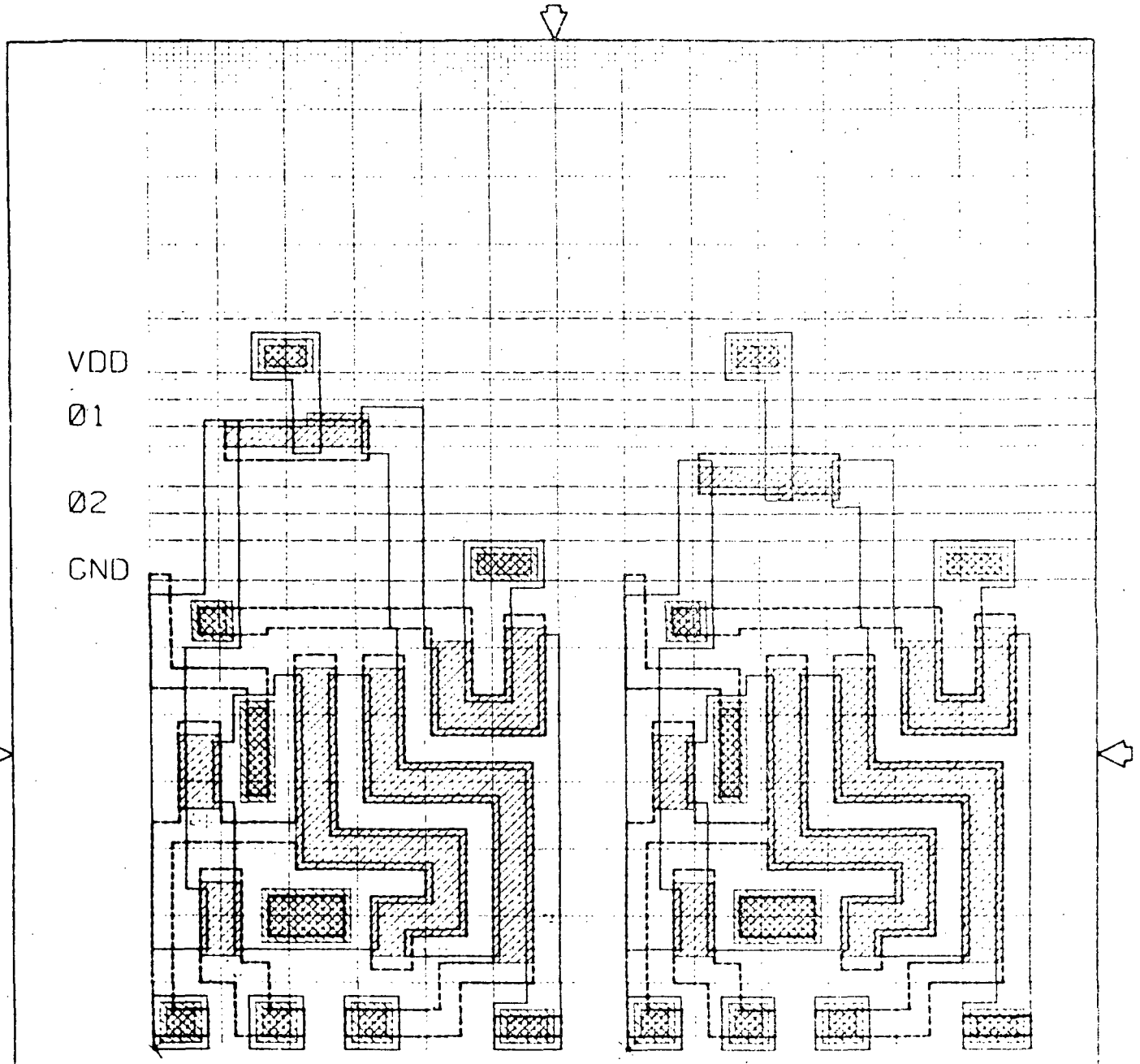
$$P = (P_{t-1}) \cdot (\bar{A} + \bar{C}) \cdot \bar{\phi}_x (B\bar{C} + \bar{A}\,[B + C])$$

FOR EXCLUSIVE OR, B = A

$$P = (P_{t-1}) \cdot (\bar{A} + \bar{C}) \cdot \bar{\phi}_x + (A\bar{C} + \bar{A}C) \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_C	2	1050	1050
C_B	3	190	190
C_A	4	820	820
C_P	5	500	470
PATTERN NO.		4350	4360



4350 **4360**

SIZE	CODE IDENT.NO.	DWG.NO.	3 INPUT DATA SWITCH (Opt. Excl. OR)
A	98230		
SCALE 0.1mil/div			

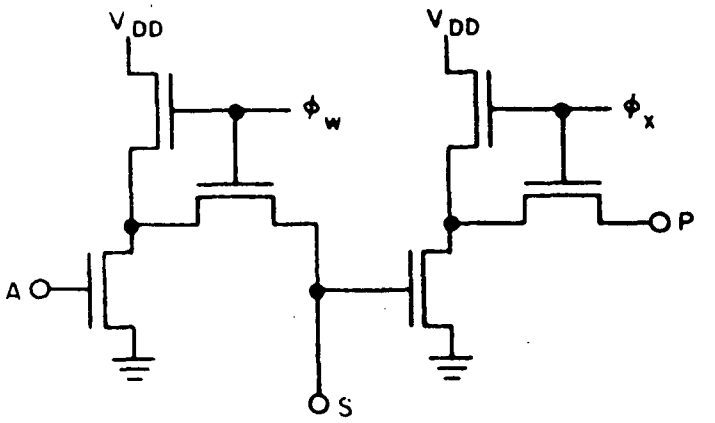
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 4pF
WITH ½ BIT AND 1 BIT DELAY OUTPUTS

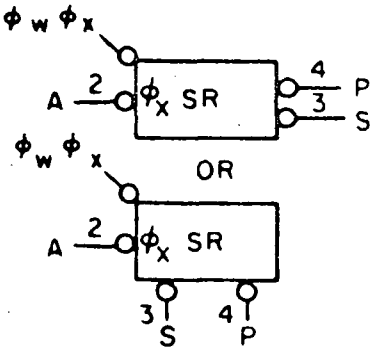
PATTERN NO. 4370 ($\phi_2\phi_1$)
4380 ($\phi_1\phi_2$)

APRIL 1968

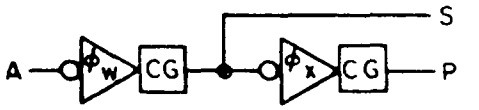
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	ϕ_w	ϕ_x	S	P
*	0	1	$\overline{A_{t-1}}$	$\overline{S_{t-1}}$
1	1	0	0	P_{t-1}
0	1	0	1	P_{t-1}

*MEANS EITHER STATE

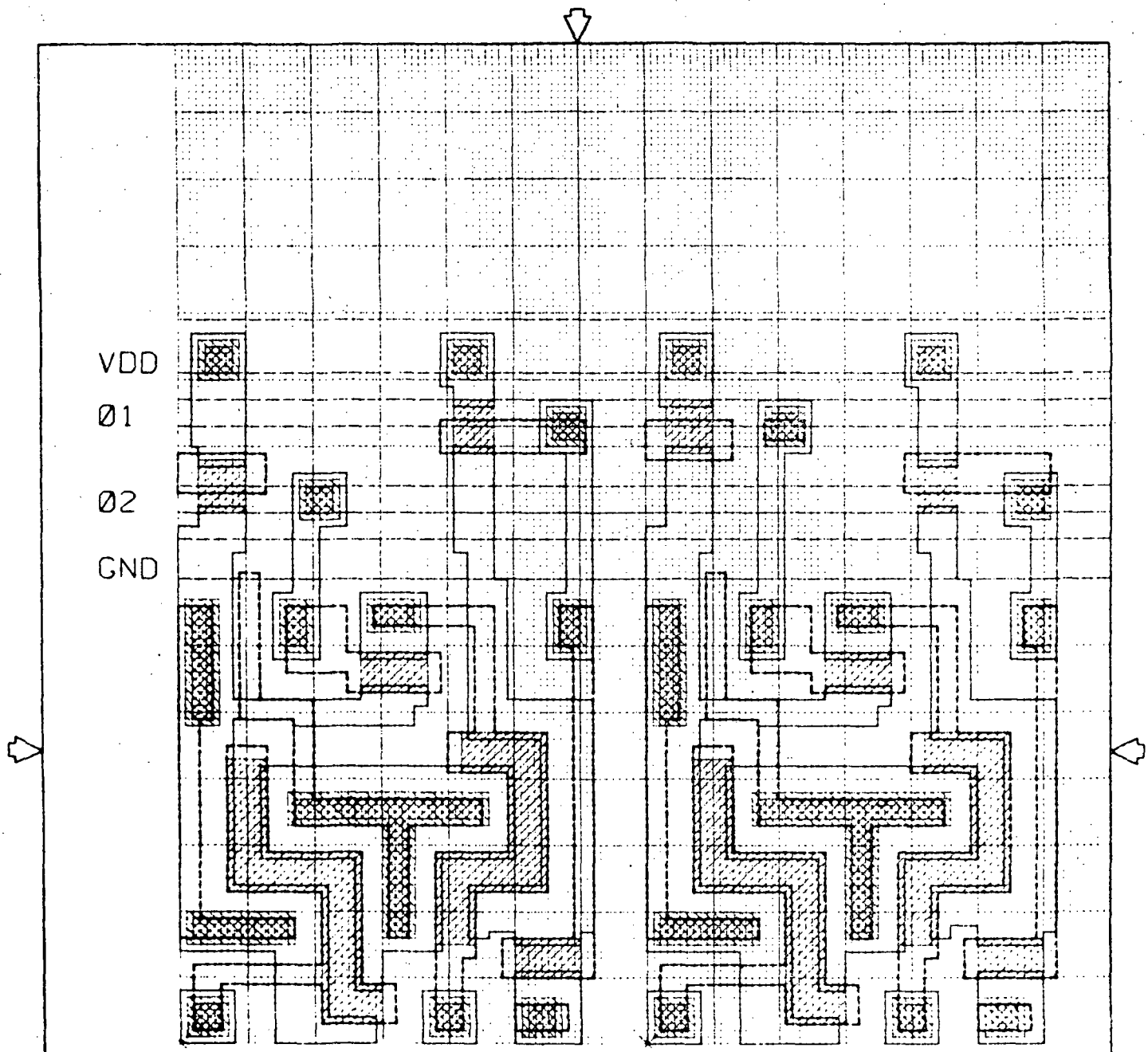
LOGIC EQUATIONS

$$S = \overline{(A_{t-1})} \cdot \phi_x + \bar{A} \cdot \phi_w$$

$$P = S_{t-1} \cdot \phi_x + P_{t-1} \cdot \phi_w$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	750	750
C_S	3	670	670
C_P	4	430	400
PATTERN NO.		4370	4380



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	DYNAMIC REGISTER STAGE Q, $\bar{Q}$ — OUTPUT	
SCALE 0.1 mil/div			SHEET

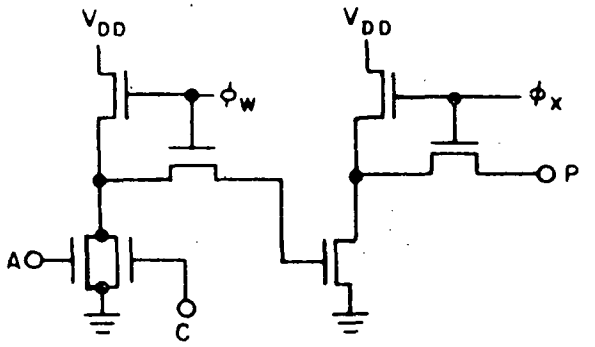
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 4pF
1 BIT DELAY OUTPUT, WITH SET

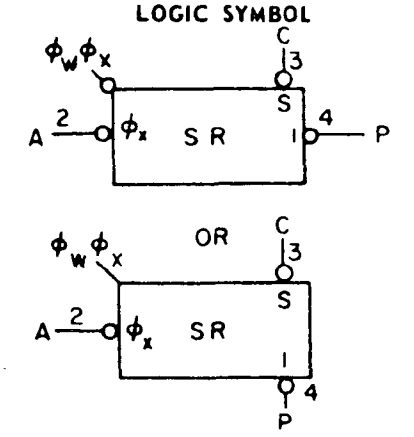
PATTERN NO. 4390 ($\phi_2\phi_1$)
4400 ($\phi_1\phi_2$)

APRIL 1968

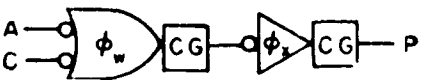
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A + C	ϕ_w	ϕ_x	P
·	0	1	$(A+C)_{t-1}$
·	1	0	P_{t-1}

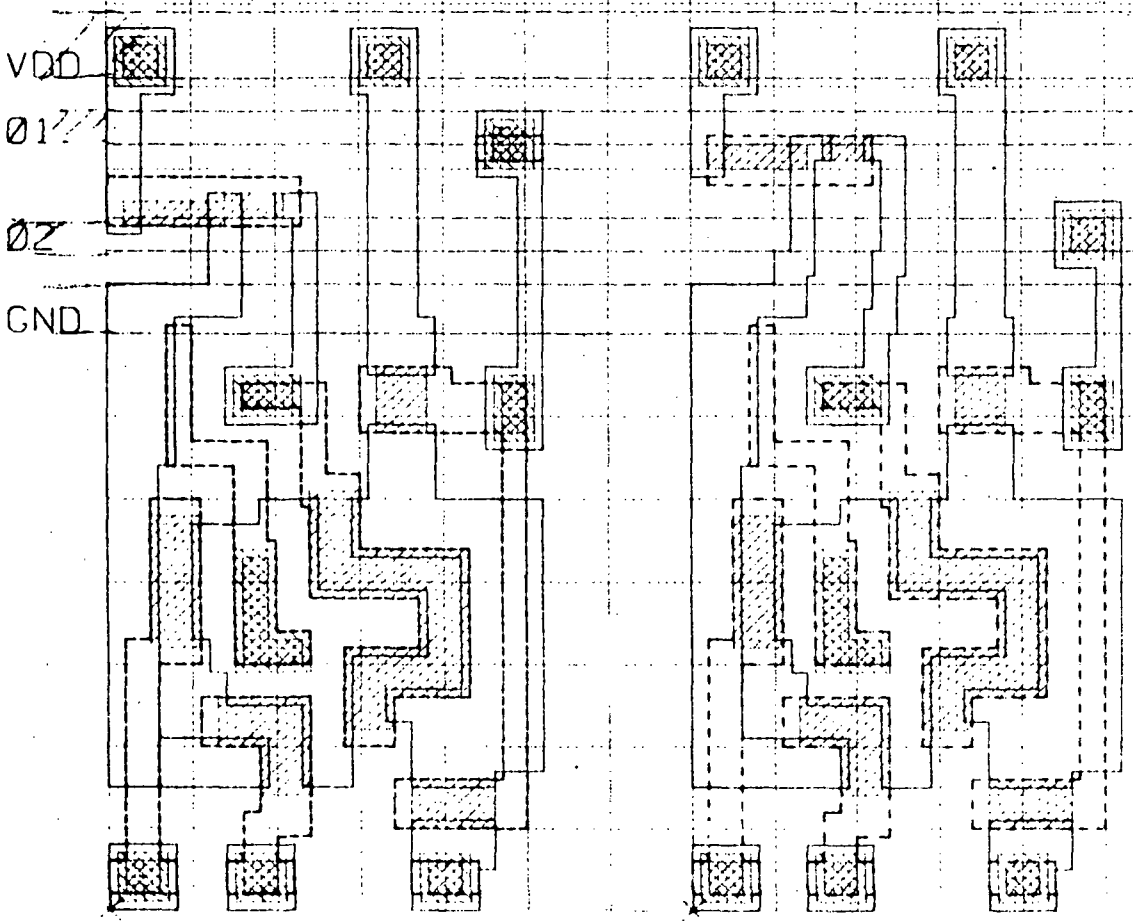
·MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (A + C)_{t-1} \cdot \phi_x + (P_{t-1}) \cdot \phi_w$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	260	260
C_C	3	260	260
C_P	4	380	380
PATTERN NO.		4390	4400



4390 4400

SIZE	CODE IDENT. NO.	DWG. NO.
A	98230	DYNAMIC REGISTER Q OUTPUT W/SET
SCALE 0.1mil/div		SHEET

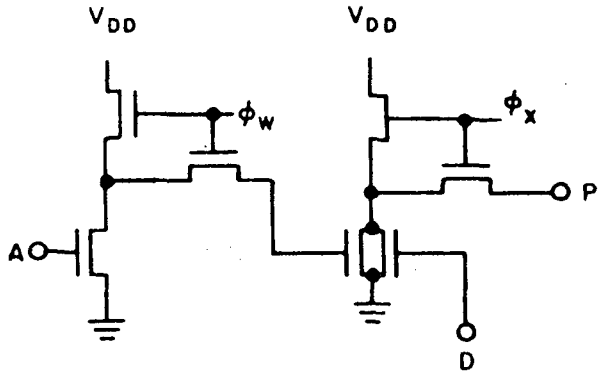
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 4pF
1 BIT DELAY OUTPUT, WITH RESET

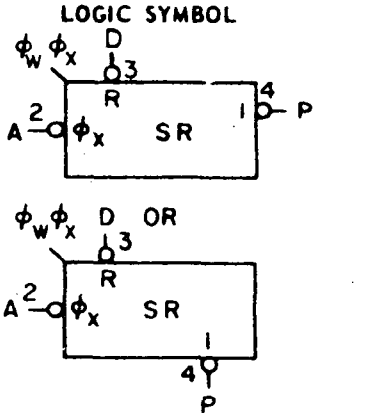
PATTERN NO. 4410 ($\phi_2\phi_1$)
4420 ($\phi_1\phi_2$)

APRIL 1968

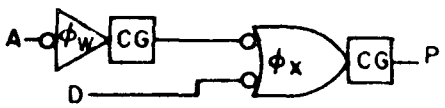
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	D	ϕ_W	ϕ_X	P
*	0	0	1	A_{t-1}
*	*	1	0	P_{t-1}
*	1	0	1	0

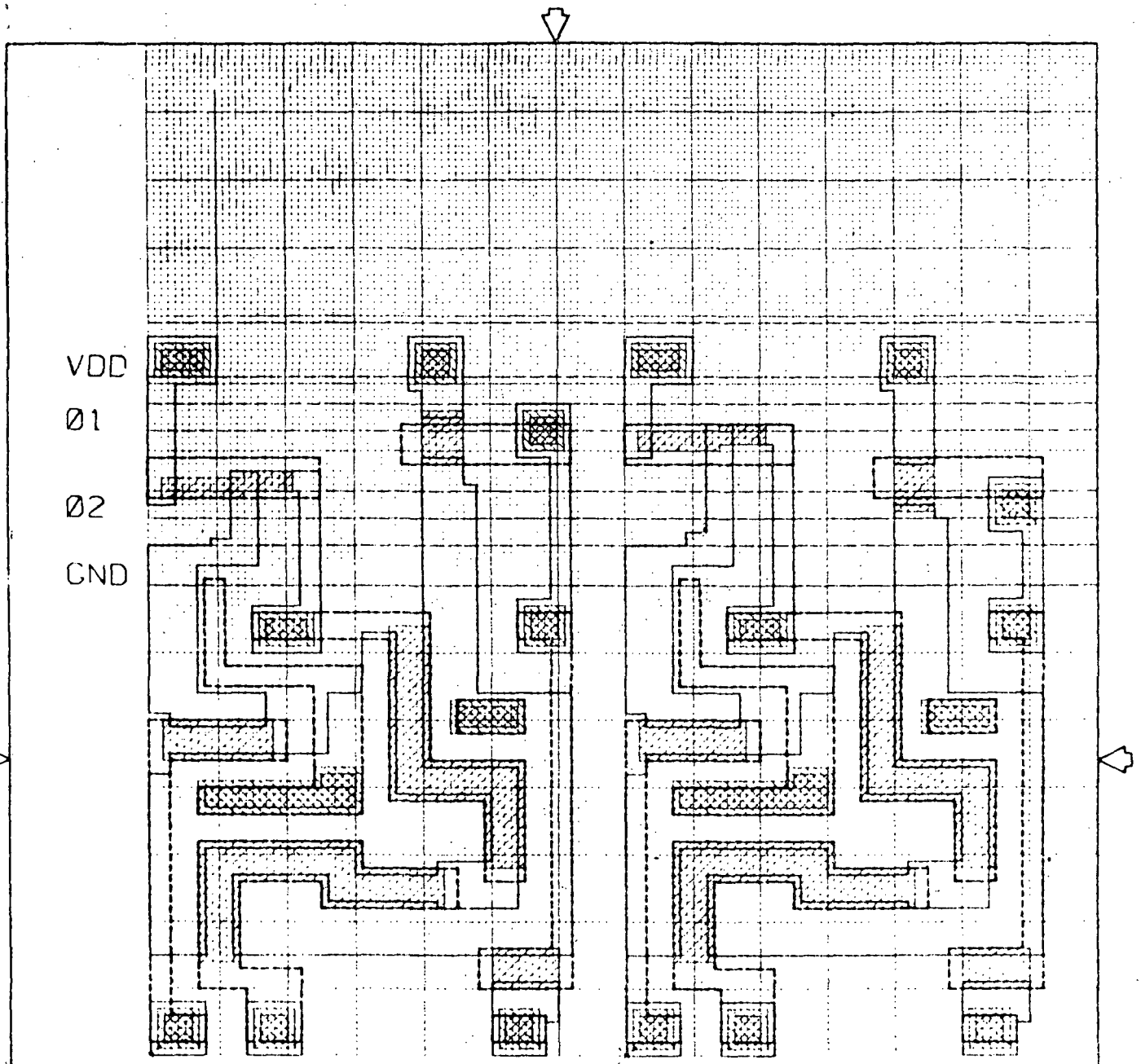
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \phi_W + (A_{t-1}) \cdot \bar{D} \cdot \phi_X$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	270	270
C_D	3	590	690
C_P	4	660	630
PATTERN NO.		4410	'20



4410 4420

SIZE	CODE IDENT NO.	DWG NO.	
A	98230	DYNAMIC REG. Q OUT W/RESET	
SCALE 0.1 mil/div			SHEET

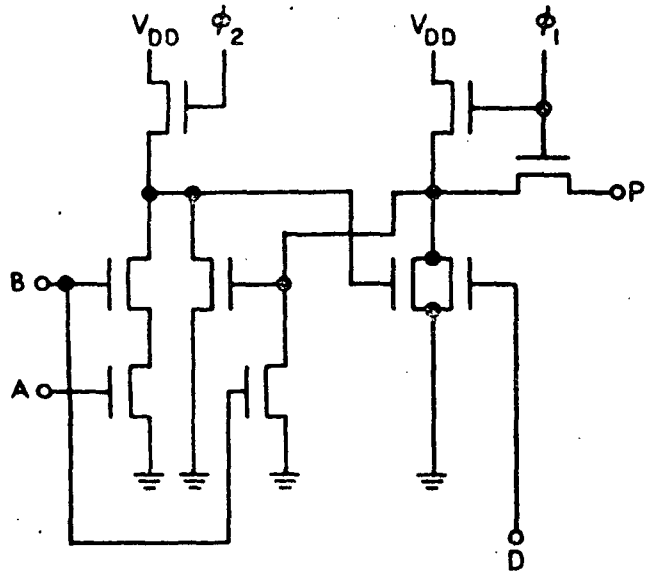
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF, "1" OUTPUT W/RESET, W/O INT. C.G.

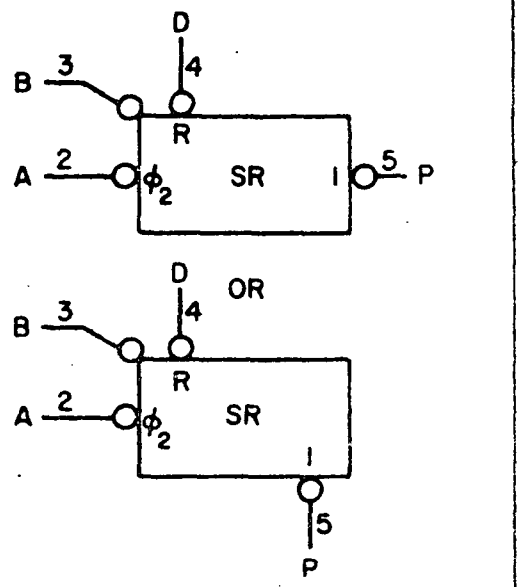
PATTERN NO. 4430(ϕ_1)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A_{t-1}	B_{t-1}	D_{t-1}	ϕ_2	D	B	ϕ_1	P
*	*	*	*	*	*	0	P_{t-1}
*	0	0	0	0	0	1	P_{t-1}
*	0	1	0	0	0	1	0
0	*	1	0	0	0	1	0
0	1	*	0	0	0	1	0
*	*	*	0	1	0	1	0
1	1	*	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_1 B MUST EQUAL ZERO

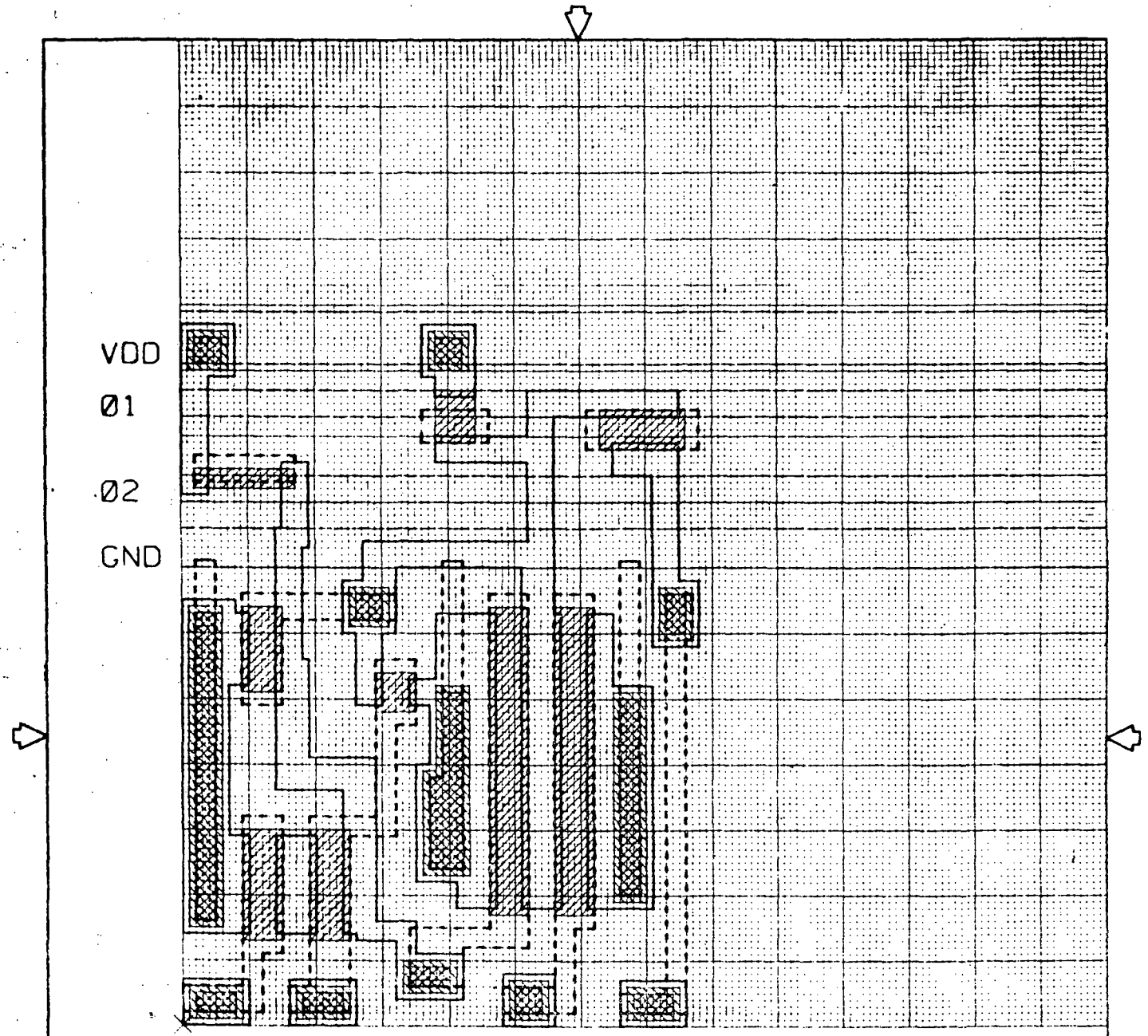
LOGIC EQUATIONS

$$P = [(A \cdot B)_{t-1} + (\overline{B} \cdot \overline{D})_{t-1} \cdot P_{t-1}] \cdot \overline{B} \cdot \overline{D} \cdot \phi_1 + P_{t-1} \cdot \overline{\phi_1}$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	260
C_B	3	350
C_D	4	620
C_P	5	700
PATTERN NO.		4430

STATIC REGISTER, "1" OUTPUT • 4430 • JUNE 1969
W/RESET, W/O INT. C.G.



4430

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	STATIC REG. Q OUTPUT W/RESET W/O INT. CG
SCALE 0.1mil/div		SHEET

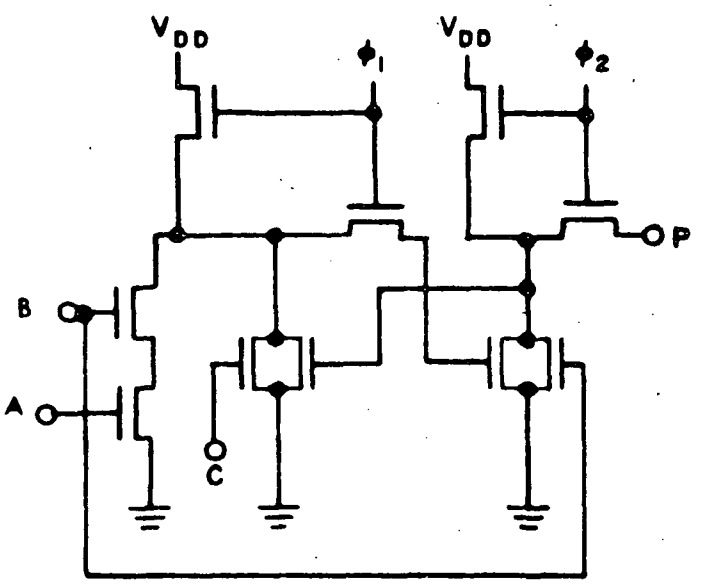
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"1" OUTPUT WITH SET

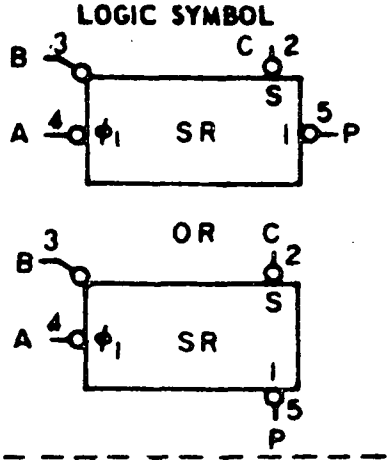
PATTERN NO. 4440 [ϕ_1 ϕ_2]

JUNE 1969

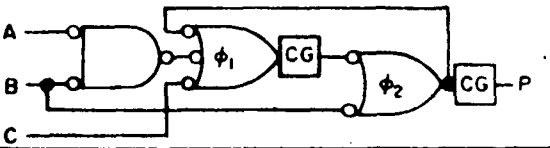
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	C_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	*	0	P_{t-1}
*	0	0	0	0	1	P_{t-1}
0	1	0	0	0	1	0
*	*	1	0	0	1	1
1	1	*	0	0	1	1

*MEANS EITHER STATE

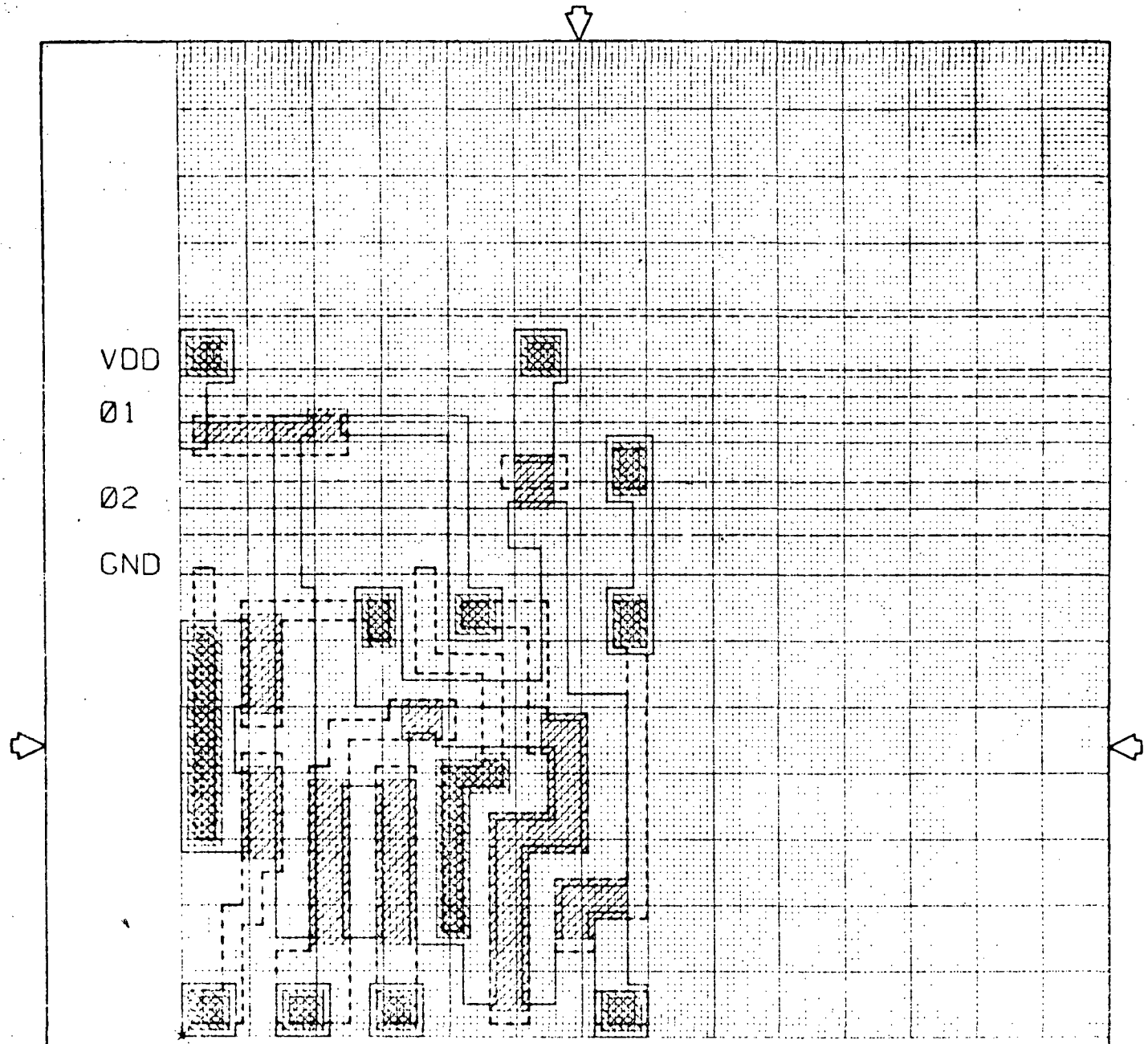
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P_t = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B}\,[A_{t-1}\,B_{t-1} + C_{t-1} + \overline{B_{t-1}}\;\overline{C_{t-1}}\;P_{t-1}]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	2	230
C_A	4	360
C_B	3	450
C_P	5	640
PATTERN NO.		4440



4440

SIZE	CODE IDENT. NO.	DWG. NO.	
A	98230		STATIC REGISTER Q OUTPUT W/SET
SCALE 0.1mil/div			SHEET

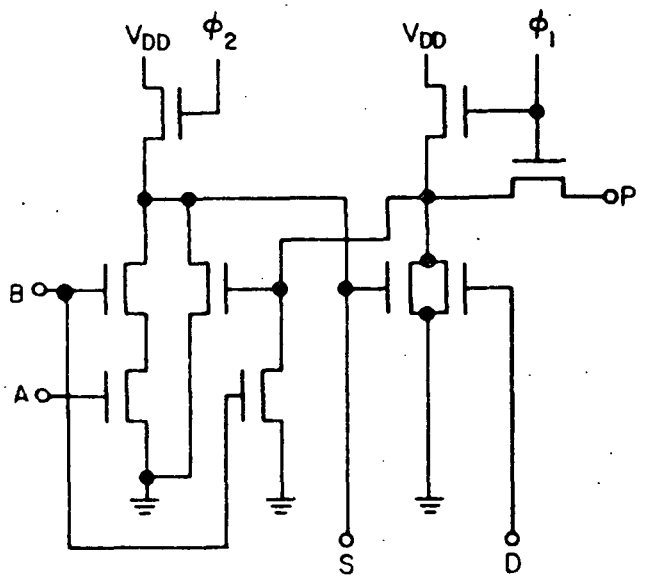
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF, "0" AND "1" OUTPUTS W/RESET, W/O INT. C.G.

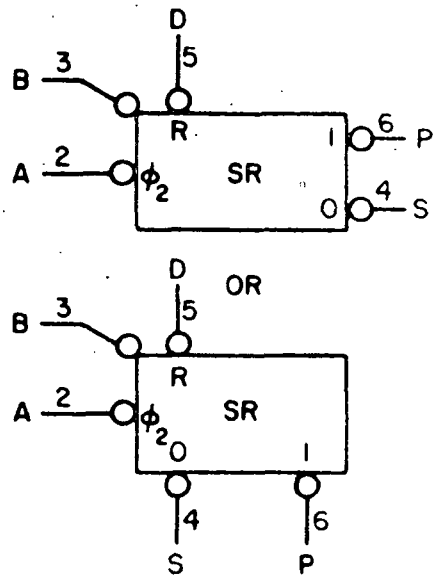
PATTERN NO. 4450(ϕ_1)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	D	ϕ_2	S	ϕ_1	P
·	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
·	0	1	1	1	0	P_{t-1}
0	·	1	1	1	0	P_{t-1}
0	1	·	1	1	0	P_{t-1}
1	1	·	·	0	0	P_{t-1}
·	0	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
·	0	1	0	·	1	0
·	0	0	0	1	1	0
·	0	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_1 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$S = [(\overline{A} + \overline{B}) \cdot D + B \cdot \overline{A} + \overline{B} \cdot \overline{D} \cdot \overline{P_{t-1}}] \cdot \phi_2$$

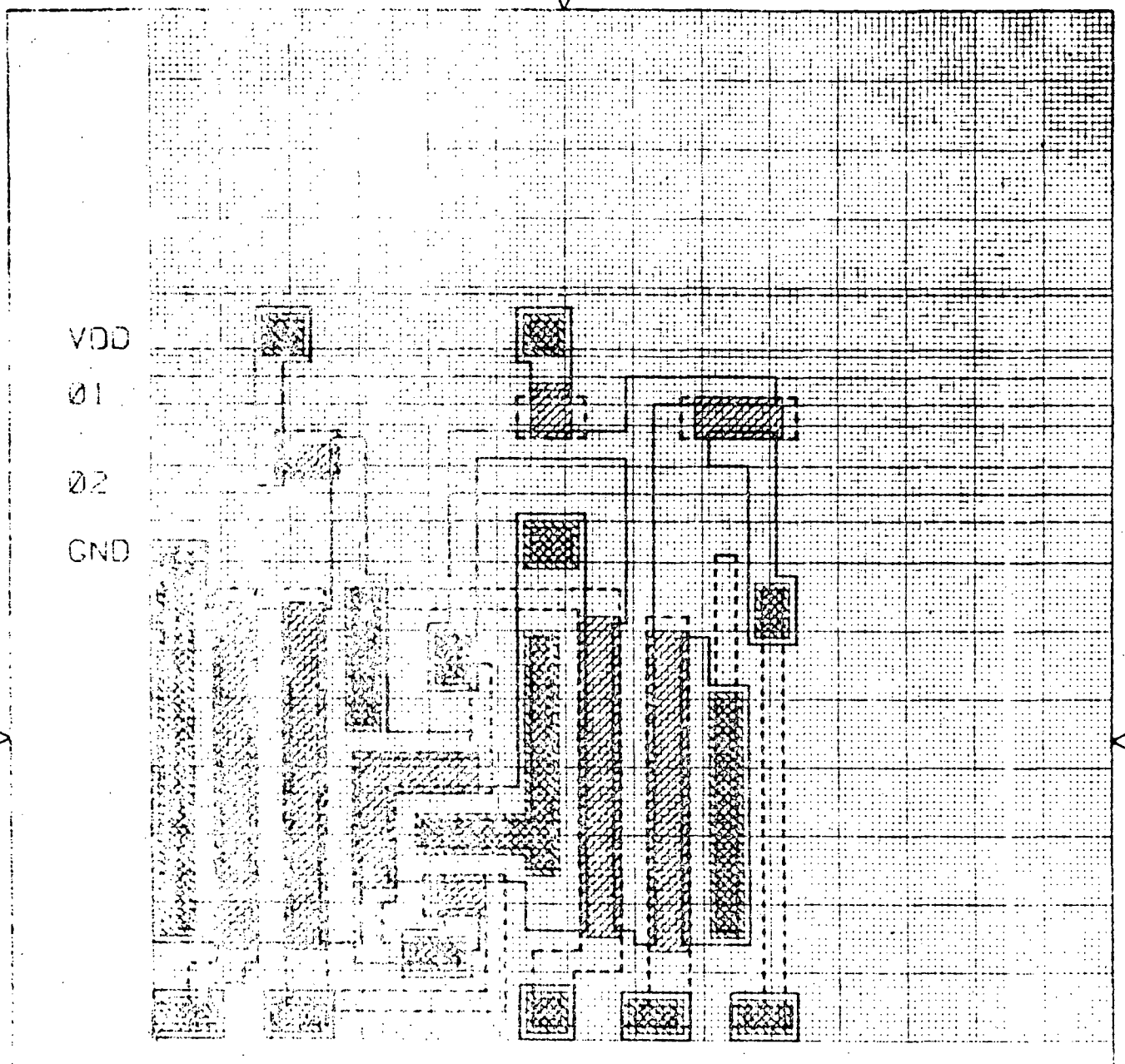
$$P = \overline{S_{t-1}} \cdot \overline{D} \cdot \overline{B} \cdot \phi_1 + P_{t-1} \cdot \overline{\phi_1}$$

$$= [(A \cdot B)_{t-1} + (\overline{B} \cdot \overline{D})_{t-1} \cdot P_{t-1}] \cdot \overline{B} \cdot \overline{D} \cdot \phi_1 + P_{t-1} \cdot \overline{\phi_1}$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	670
C_B	3	780
C_S	4	1040
C_D	5	620
C_P	6	960
PATTERN NO.		4450

STATIC REGISTER, "0" AND "1" OUTPUTS • 4450 JUNE 1969
W RESET, W O INT. C. G.



4430

A 83230	STATIC REG. Q $\overline{Q}$ W/RESET W/O INT. CG
div	SHEET

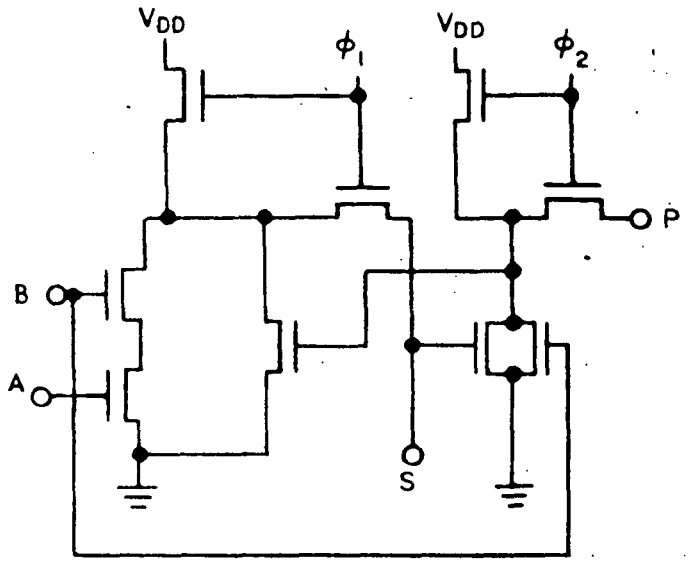
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"0" AND "1" OUTPUTS

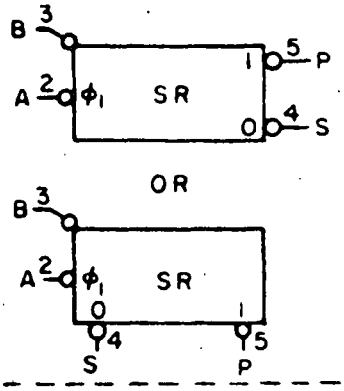
PATTERN NO. 4460 (ϕ_1 ϕ_2)

JUNE 1969

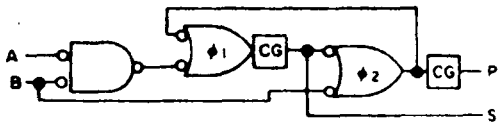
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	ϕ_1	S	ϕ_2	P
·	·	0	S_{t-1}	–	–
·	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	1	1	0	P_{t-1}
1	1	1	0	0	P_{t-1}
·	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
·	0	0	1	1	0
·	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

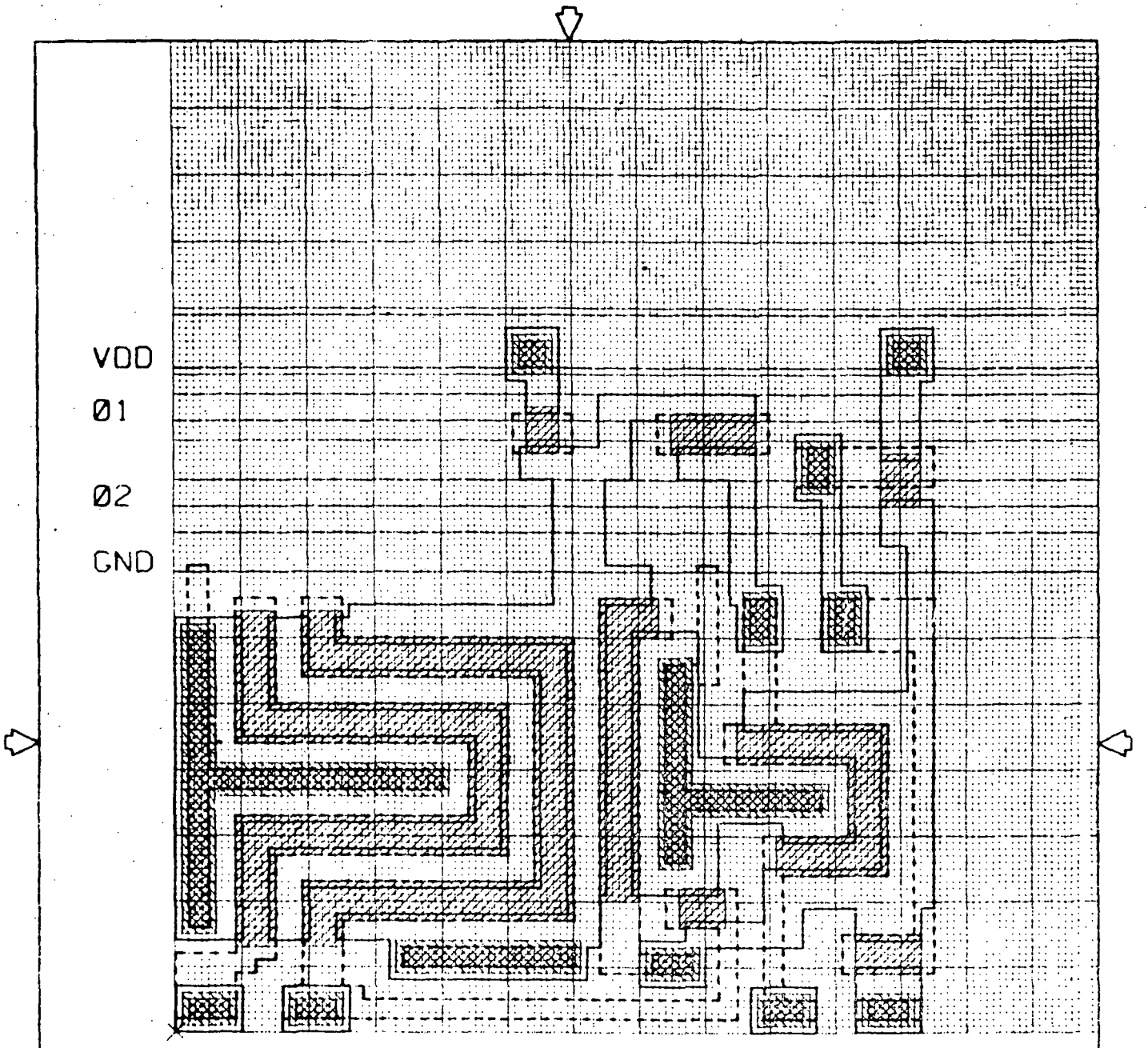
$$S = [\bar{B} \cdot \overline{P_{t-1}} + \bar{A} \cdot B]\,\phi_1 + S_{t-1} \cdot \overline{\phi_1}$$

$$P = \overline{S_{t-1}} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$= [\overline{B_{t-1}} \cdot P_{t-1} + A_{t-1} \cdot B_{t-1}]\,\phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	1520
C_B	3	1650
C_S	4	1470
C_P	5	970
PATTERN NO.		4460



4460

SIZE	CODE IDENT. NO.	DWG. NO.	STATIC REGISTER Q, $\bar{Q}$ OUTPUT
A	98230		
SCALE 0.1mil/div			SHEET

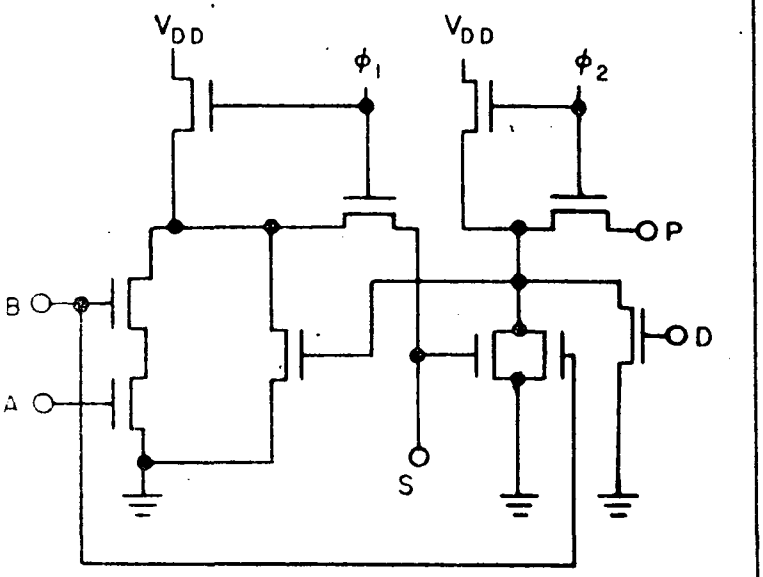
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 1F
"0" AND "1" OUTPUTS WITH RESET

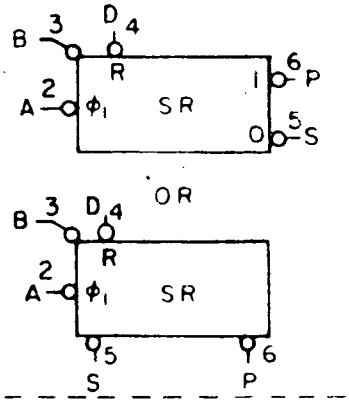
PATTERN NO. 4480 (ϕ_1, ϕ_2)

JUNE 1969

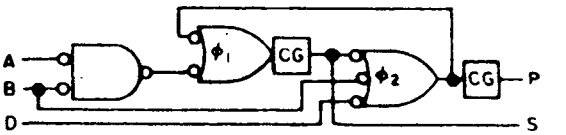
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	D	ϕ_1	S	ϕ_2	P
·	*	·	0	S_{t-1}	–	–
·	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
·	0	1	1	1	0	P_{t-1}
0	·	1	1	1	0	P_{t-1}
0	1	·	1	1	0	P_{t-1}
1	1	·	1	0	0	P_{t-1}
·	0	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
·	0	1	0	*	1	0
·	0	0	0	1	1	0
·	0	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

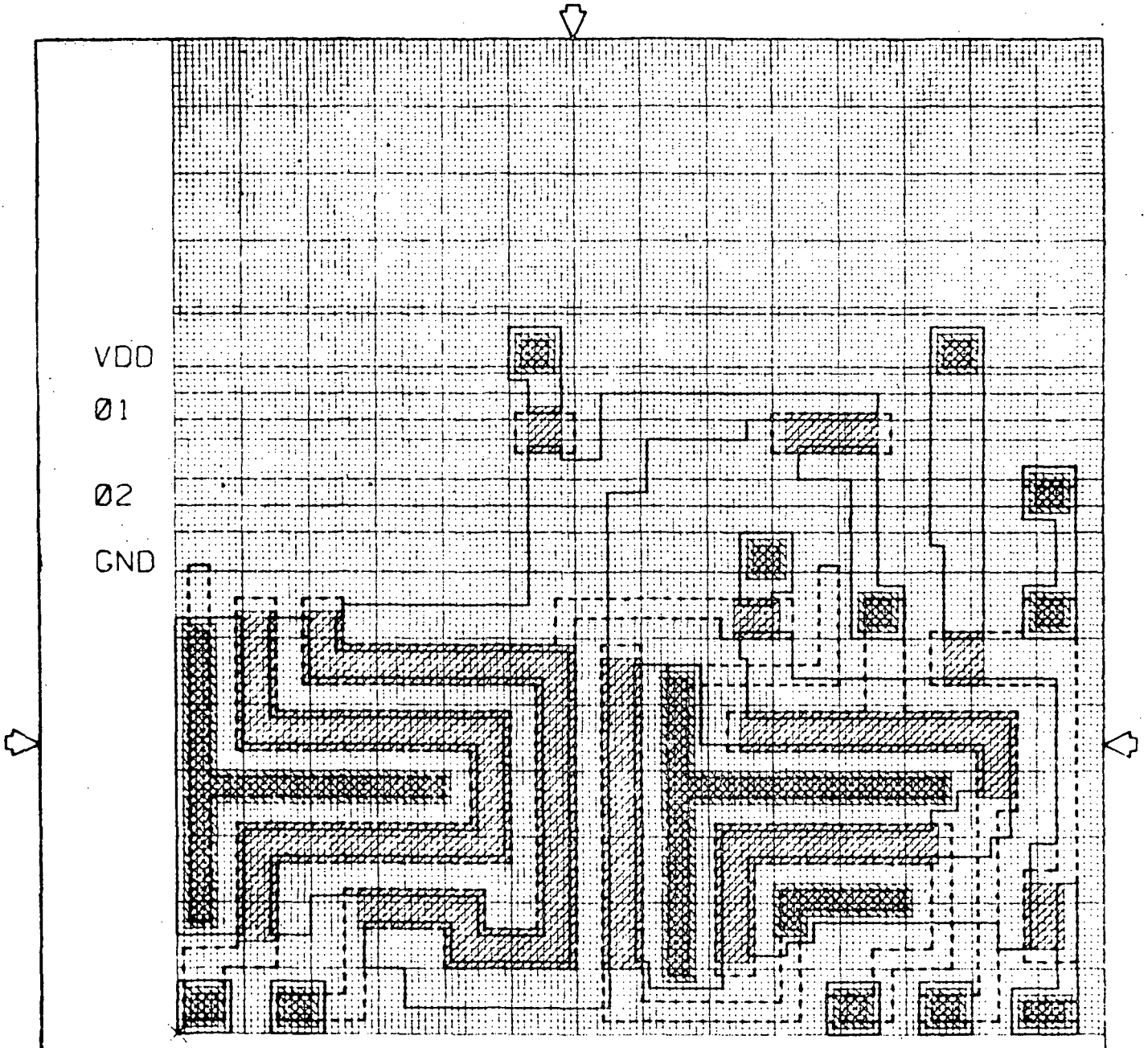
$$S = [(\bar{A} + \bar{B}) \cdot D + B \cdot \bar{A} + \bar{B} \cdot \bar{D} \cdot \overline{P_{t-1}}] \cdot \phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \overline{\phi_2}$$

$$= [A_{t-1} \cdot B_{t-1} + \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	1500
C_B	3	1630
C_D	4	660
C_S	5	1550
C_P	6	1040
PATTERN NO.		4480



4480

SIZE	CODE IDENT. NO.	DWG. NO.	
A	98230		STATIC REGISTER Q, $\bar{Q}$ OUTPUT W/ RESET
SCALE 0.1mil/div			SHEET

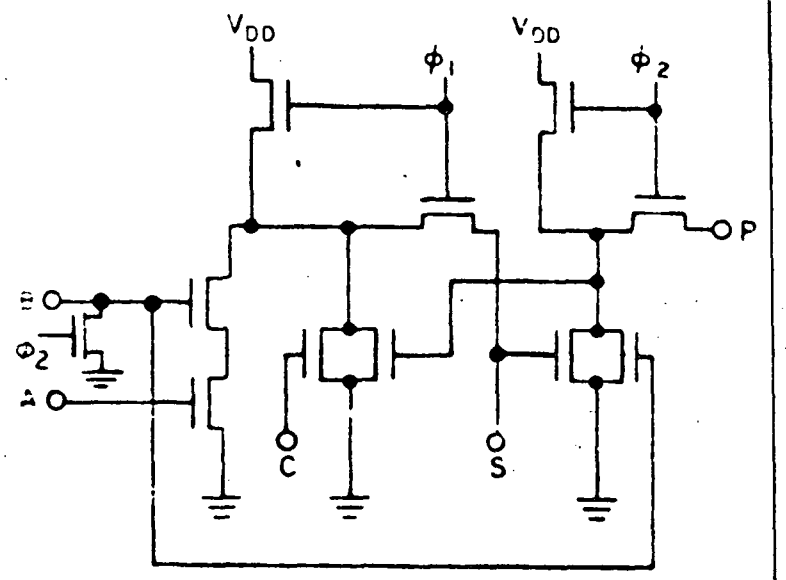
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF — PATTERN NO. 4500 [$\phi_1 \phi_2$]

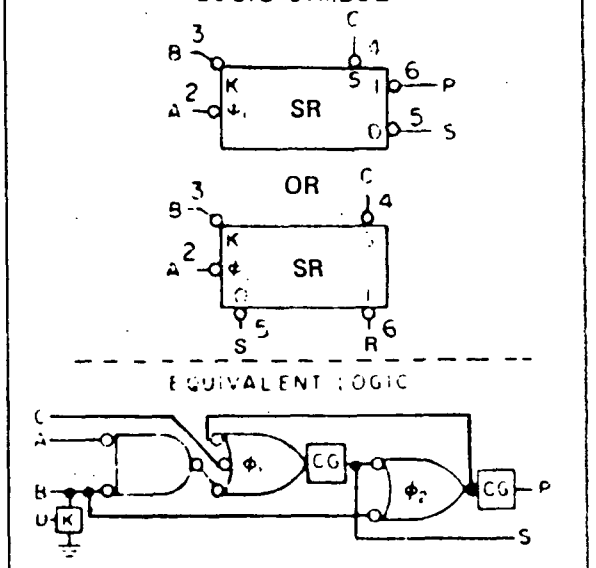
"0" AND "1" OUTPUTS, SET AND KILL

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	1	S	2	P
			0	S_{t-1}	-	-
	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	0	1	1	0	P_{t-1}
	1	1	1	0	0	P_{t-1}
1	1	*	1	0	0	P_{t-1}
	0	*	0	$\overline{P_{t-1}}$	1	P_{t-1}
	0	*	0	1	1	0
	0		0	1 0	1	

* MEANS EITHER STATE

LOGIC EQUATIONS

$$S \quad \bar{B} \cdot \bar{C} \cdot \overline{P_{t-1}} \cdot B \cdot \bar{A} \cdot \bar{C} \cdot \phi_1 \quad S_{t-1} \cdot \overline{\phi_1}$$

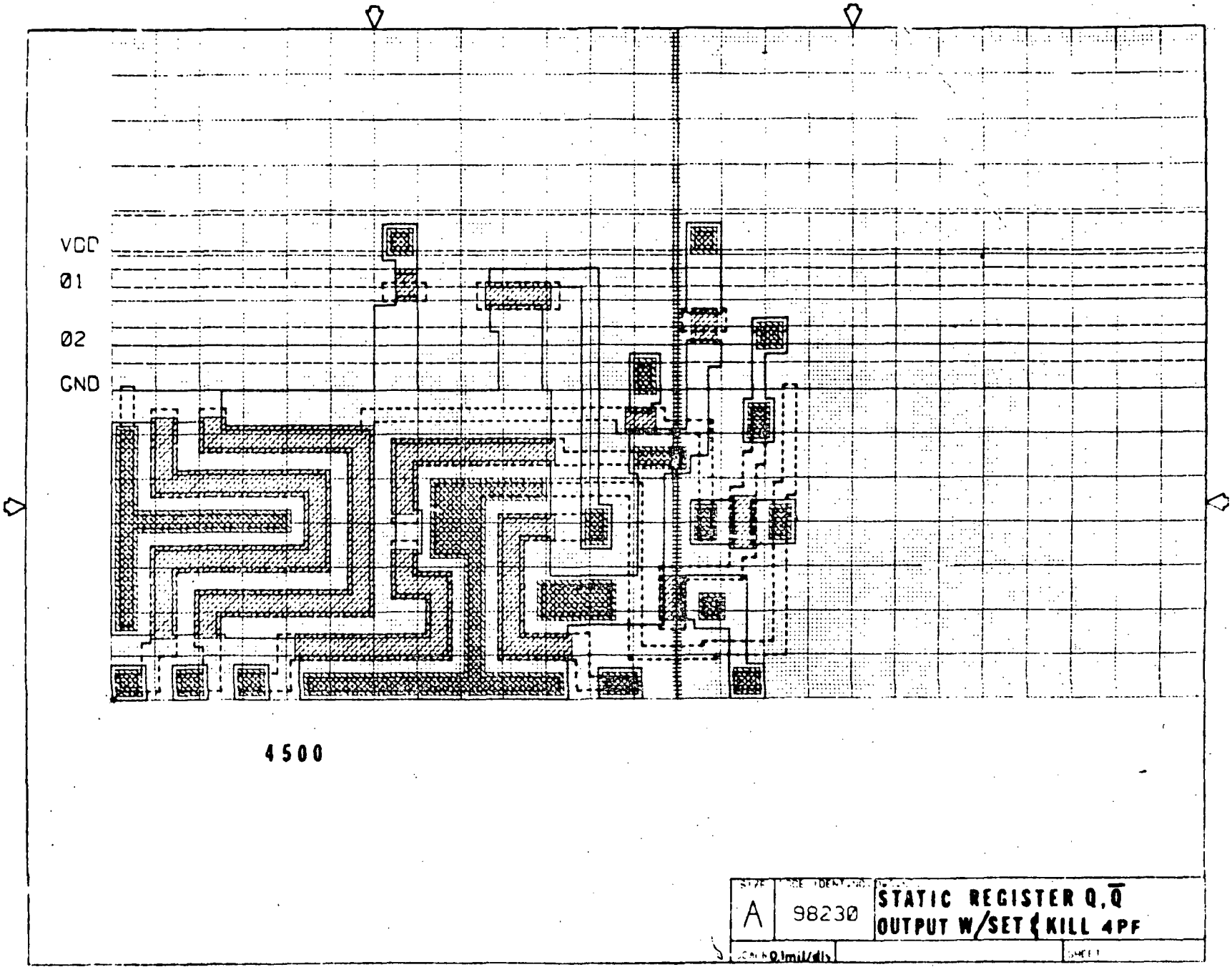
$$P \quad \overline{S_{t-1}} \cdot \phi_2 \cdot \bar{B} \cdot P_{t-1} \cdot \bar{\phi}_2$$

$$A_{t-1}\, B_{t-1} \quad C_{t-1} \quad \overline{B_{t-1}} \cdot \overline{C_{t-1}} \cdot P_{t-1} \cdot \phi_2 \cdot \bar{B}$$

$$+ P_{t-1} \cdot \bar{\phi}_2$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	4	810
C_A	2	1500
C_B	3	1700
C_S	5	1860
C_P	6	1100
PATTERN NO.		4500


VDD
Ø1
Ø2
GND
4500
SIZE
A
98230
STATIC REGISTER Q, Q̄
OUTPUT W/SET & KILL 4PF
SHEET

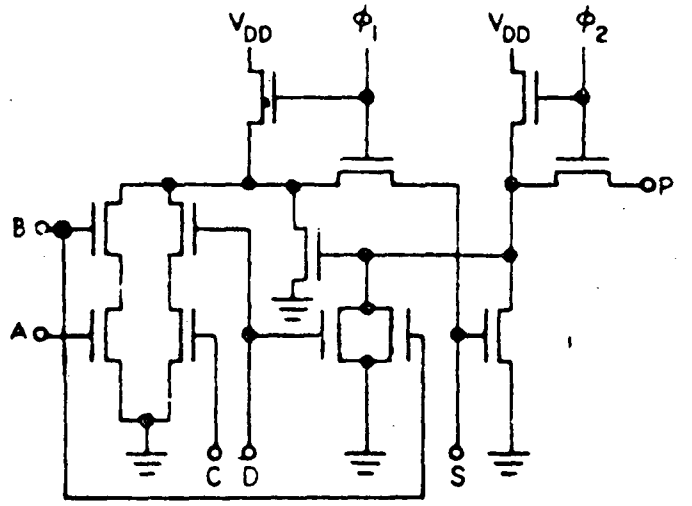
BANNING THICK OXIDE STANDARD CELL

DUAL SAMPLE REGISTER, 4pF
"0" AND "1" OUTPUTS

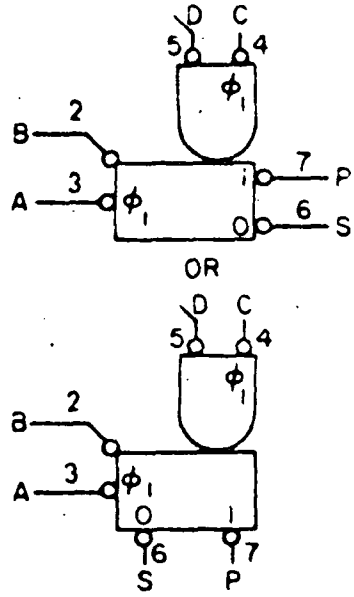
PATTERN NO. 4520 (ϕ_1 & ϕ_2)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

J	K	ϕ_1	S	D	ϕ_2	P
*	*	0	S_{t-1}	–	–	–
0	0	1	$\overline{P_{t-1}}$	0	0	P_{t-1}
1	0	1	1	*	0	P_{t-1}
*	1	1	0	*	0	P_{t-1}
0	*	0	$\overline{P_{t-1}}$	0	1	P_{t-1}
1	*	0	*	1	1	0
0	*	0	1	0	1	0
0	0	0	0	0	1	1

*MEANS EITHER STATE

B AND D ARE SAMPLE INPUTS
DURING ϕ_2 B AND D MUST EQUAL ZERO

LOGIC EQUATIONS

J = B + D

K = A · B + C · D

$$S = S_{t-1} \cdot \bar{\phi}_1 + J \cdot \bar{K} + \bar{J} \cdot \bar{K} \cdot \overline{P_{t-1}} \cdot \phi_1$$

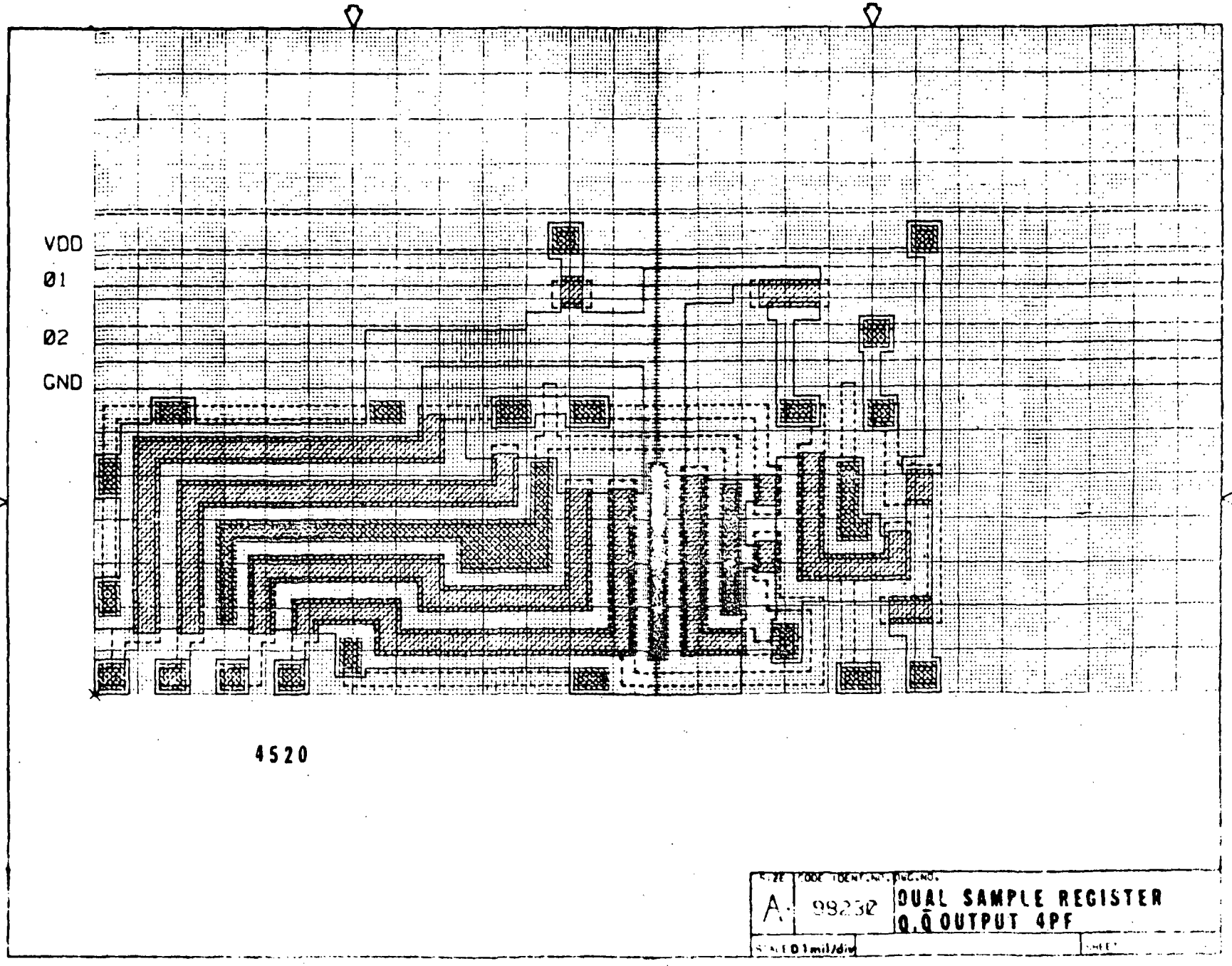
$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \bar{B} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$= K_{t-1} + \overline{J_{t-1}} \cdot \overline{K_{t-1}} \cdot P_{t-1} \cdot \bar{D} \cdot \bar{B} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	1420
C_B	2	1690
C_C	4	1500
C_D	5	1630
C_S	6	2640
C_P	7	850
PATTERN NO.		4520

DUAL SAMPLE REGISTER • 4520 • JUNE 1969
"0" AND "1" OUTPUTS


VDD
Ø1
Ø2
GND
4520
A
98230
DUAL SAMPLE REGISTER
Q,Q̄ OUTPUT 4PF

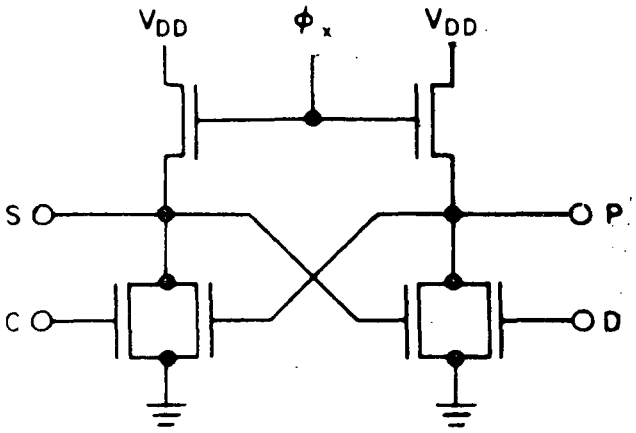
BANNING THICK OXIDE STANDARD CELL

RS FLIP FLOP, NO DELAY, 4pF
"0" AND "1" OUTPUTS

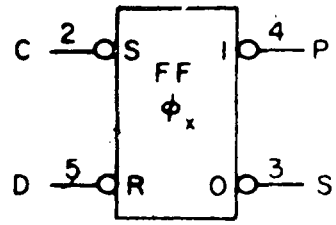
PATTERN NO. 4530 (ϕ_1)
4540 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

D	C	ϕ_x	S	P
0	0	*	S_{t-1}	P_{t-1}
0	1	0	0	P_{t-1}
1	0	0	S_{t-1}	0
0	1	1	0	1
1	0	1	1	0

*MEANS EITHER STATE

C AND D ARE MUTUALLY EXCLUSIVE

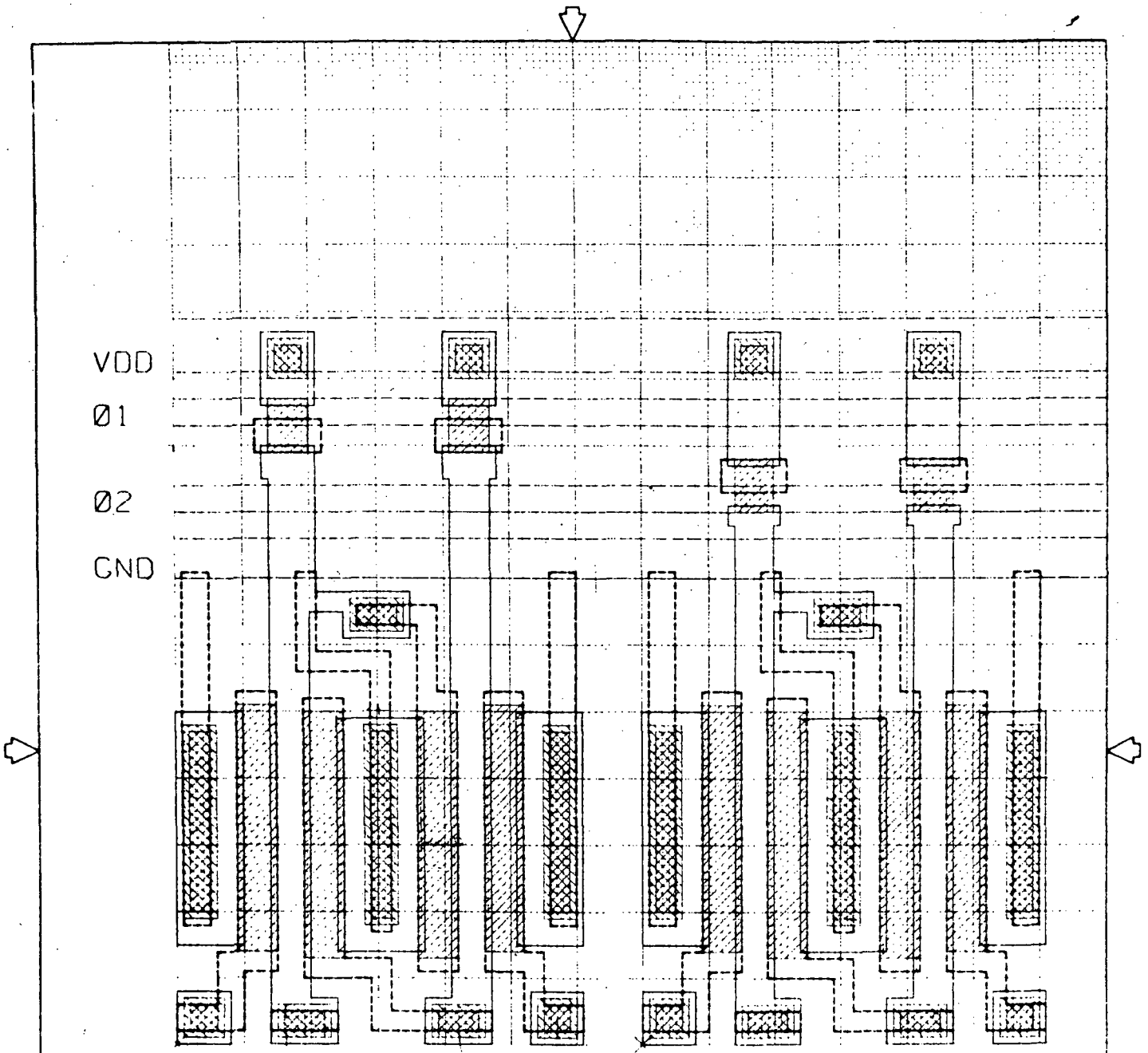
LOGIC EQUATIONS

$$S = S_{t-1}(\bar{D} \cdot \bar{C} + D \cdot \bar{C} \cdot \bar{\phi}_x) + D \cdot \phi_x$$

$$P = P_{t-1}(\bar{D} \cdot \bar{C} + \bar{D} \cdot C \cdot \bar{\phi}_x) + C \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_C	2	500	500
C_S	3	880	820
C_P	4	870	830
C_D	5	500	500
PATTERN NO.		4530	4540



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	RSFF NO DELAY Q, $\bar{Q}$ OUTPUT
SCALE 0.1mil/div		SHEET

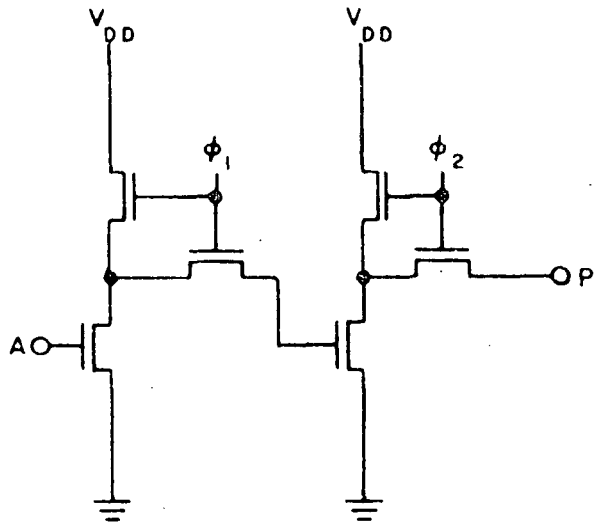
BANNING THICK OXIDE STANDARD CELL

DYNAMIC SHIFT REGISTER, 4pF .
1 BIT DELAY OUTPUT

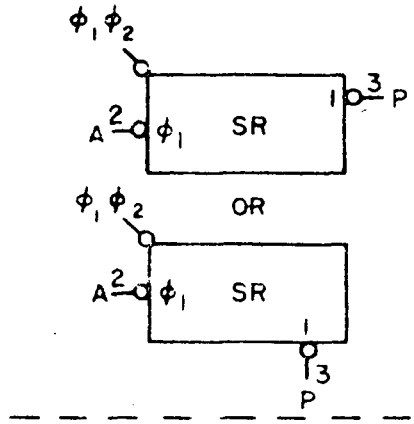
PATTERN NO. 4580 (ϕ_1 ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_1	ϕ_2	P
*	0	1	A_{t-1}
*	1	0	P_{t-1}

*MEANS EITHER STATE

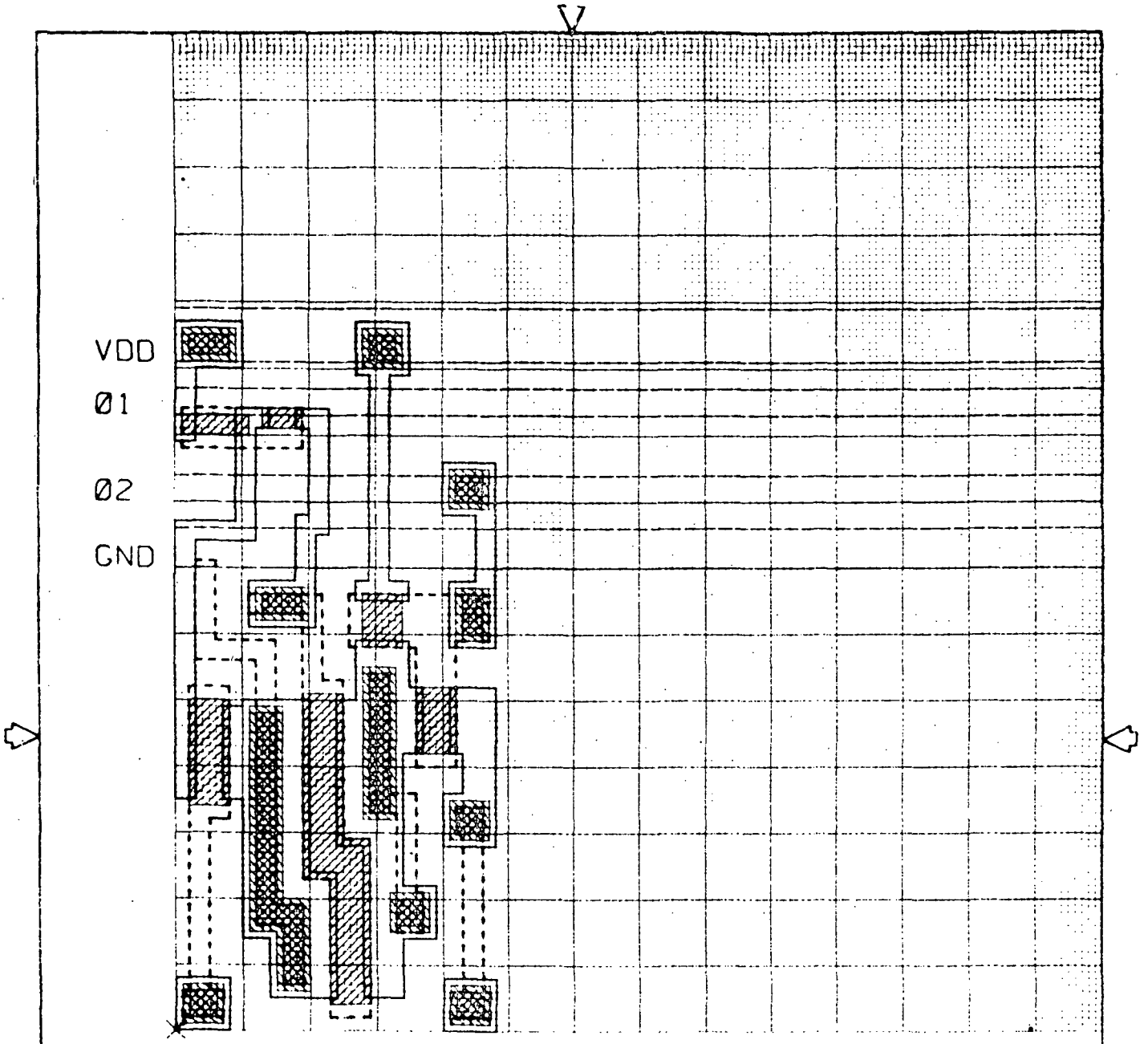
LOGIC EQUATIONS

$$P = (A_{t-1}) \cdot \phi_2 + (P_{t-1}) \cdot \phi_1$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	260
C_P	3	450
PATTERN NO.		4580

DYNAMIC SHIFT REGISTER • 4580 • APRIL 1968
1 BIT DELAY OUTPUT



4580

SIZE	CODE IDENT. NO.	DWG. NO.	
A	98230	DYNAMIC REGISTER Q OUT	
SCALE 0.1mil/div			SHEET

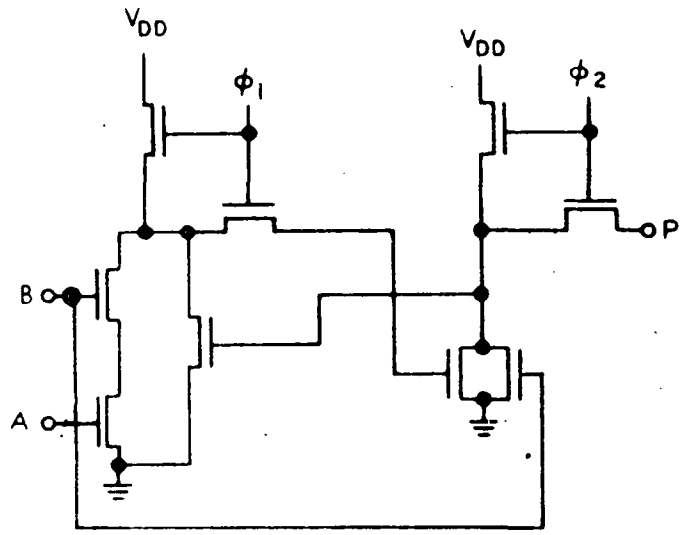
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"1" OUTPUT

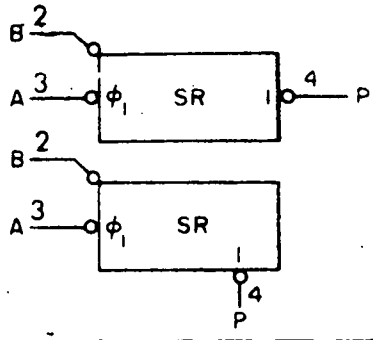
PATTERN NO. 4600 (ϕ_1 ϕ_2)

JUNE 1969

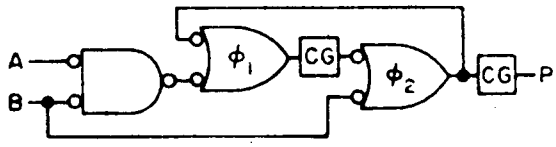
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

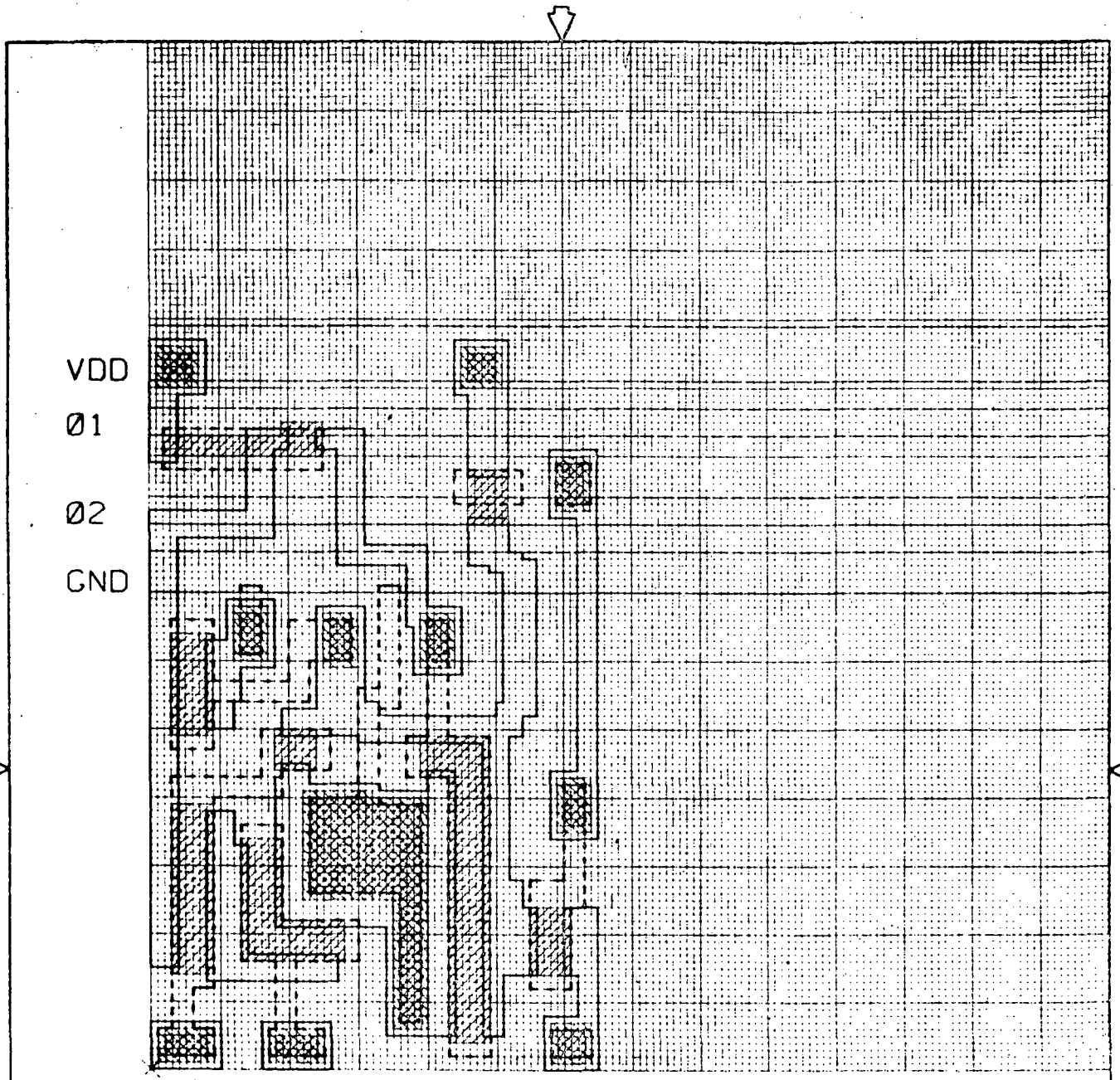
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B} \left[A_{t-1} B_{t-1} + \overline{B_{t-1}} P_{t-1} \right]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	380
C_B	2	440
C_P	4	570
PATTERN NO.		4600



4600

SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REGISTER Q OUTPUT
A	98230		
SCALE 0.1 mil/div			SHEET

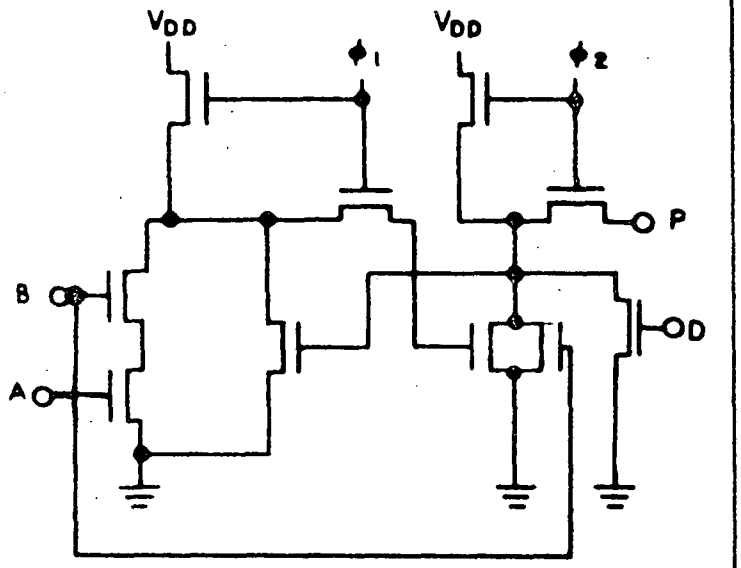
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"1" OUTPUT WITH RESET

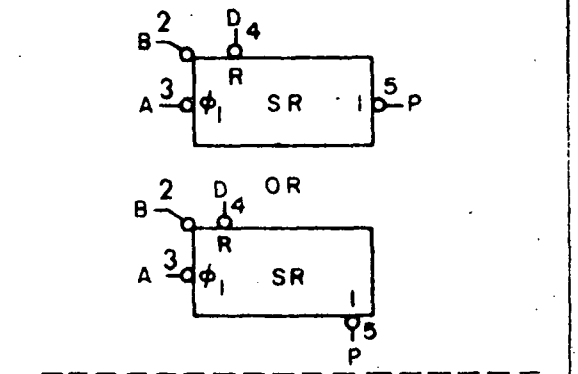
PATTERN NO. 4620 (ϕ_1 ϕ_2)

JUNE 1969

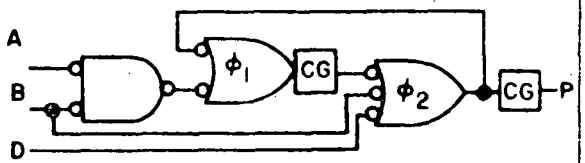
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	D_{t-1}	ϕ_1	D	B	ϕ_2	P
*	*	*	*	*	*	0	P_{t-1}
*	0	0	0	0	0	1	P_{t-1}
*	0	1	0	0	0	1	0
0	*	1	0	0	0	1	0
0	1	*	0	0	0	1	0
*	*	*	0	1	0	1	0
1	1	*	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

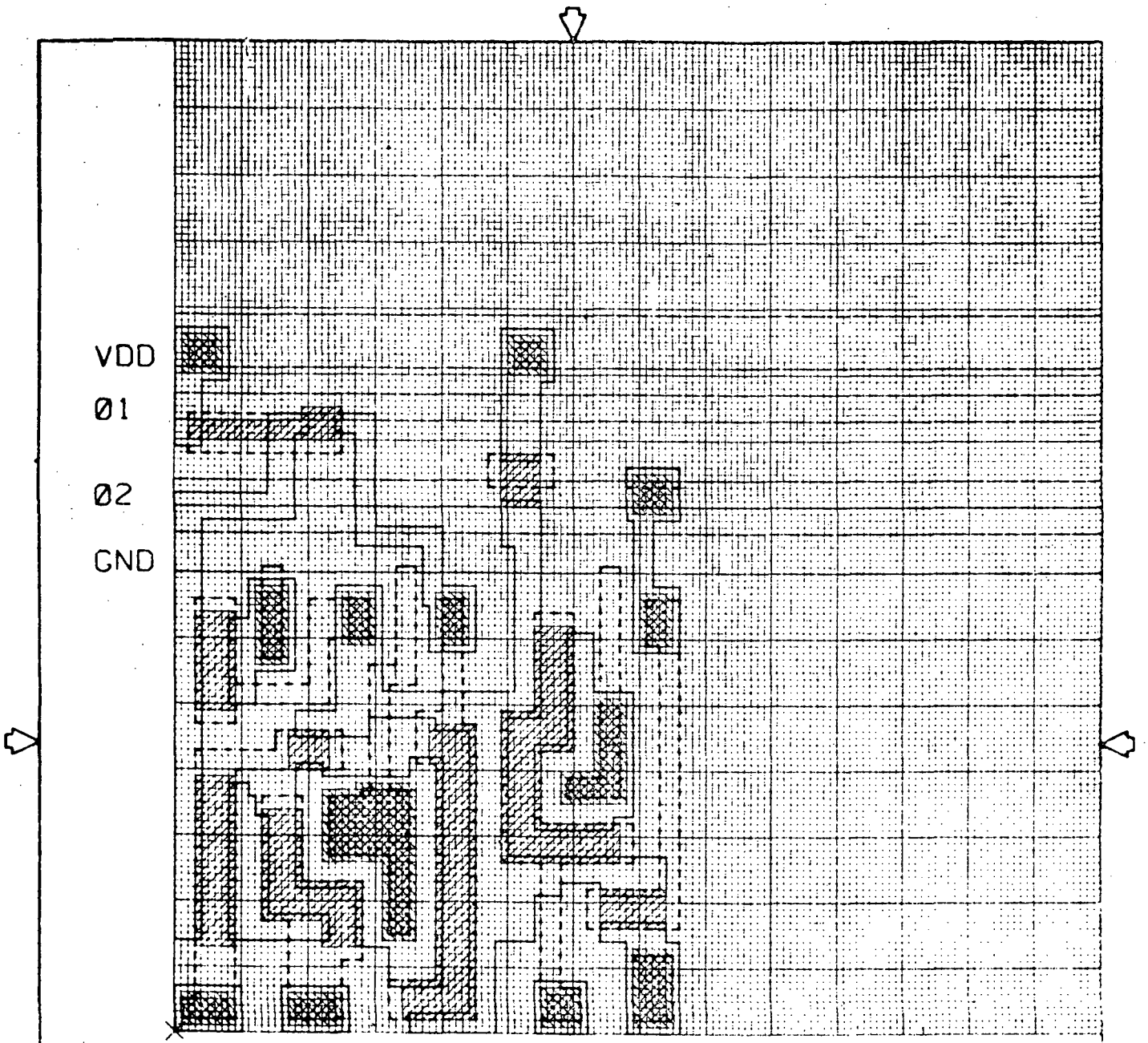
LOGIC EQUATIONS

$$P = [A_{t-1} \cdot B_{t-1} + \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	3	430
C_B	2	450
C_D	4	700
C_P	5	700
PATTERN NO.		4620

STATIC REGISTER, 4pF • 4620 • JUNE 1969
"1" OUTPUT WITH RESET



4620

SIZE	CODE IDENT.NO.	DWG.NO.	STATIC REGISTER Q OUTPUT W/RESET
A	98230		
SCALE 0.1mil/div			SHEET

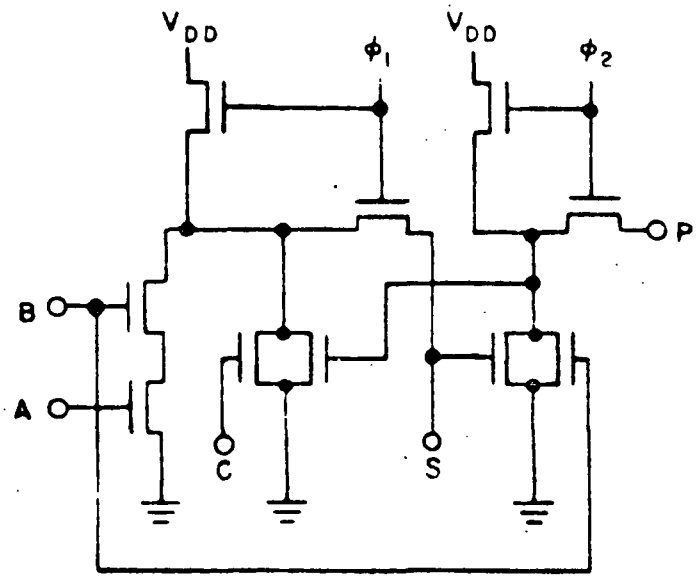
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"0" AND "1" OUTPUTS WITH SET

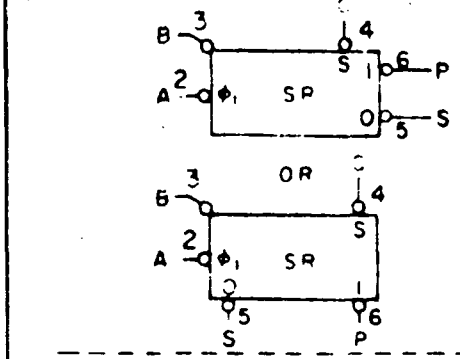
PATTERN NO. 4640 (ϕ_1 ϕ_2)

JUNE 1969

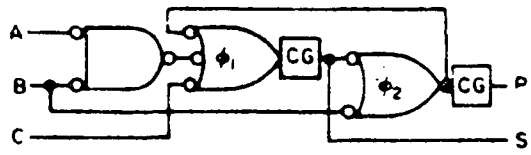
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A	B	C	ϕ_1	S	ϕ_2	P
*	*	*	0	S_{t-1}	-	-
*	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	0	1	1	0	P_{t-1}
*	*	1	1	0	0	P_{t-1}
1	1	*	1	0	0	P_{t-1}
*	0	*	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	*	0	1	1	0
*	0	*	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$S = [\bar{B} \cdot \bar{C} \cdot \overline{P_{t-1}} + B \cdot \bar{A} \cdot \bar{C}] \cdot \phi_1 + S_{t-1} \cdot \overline{\phi_1}$$

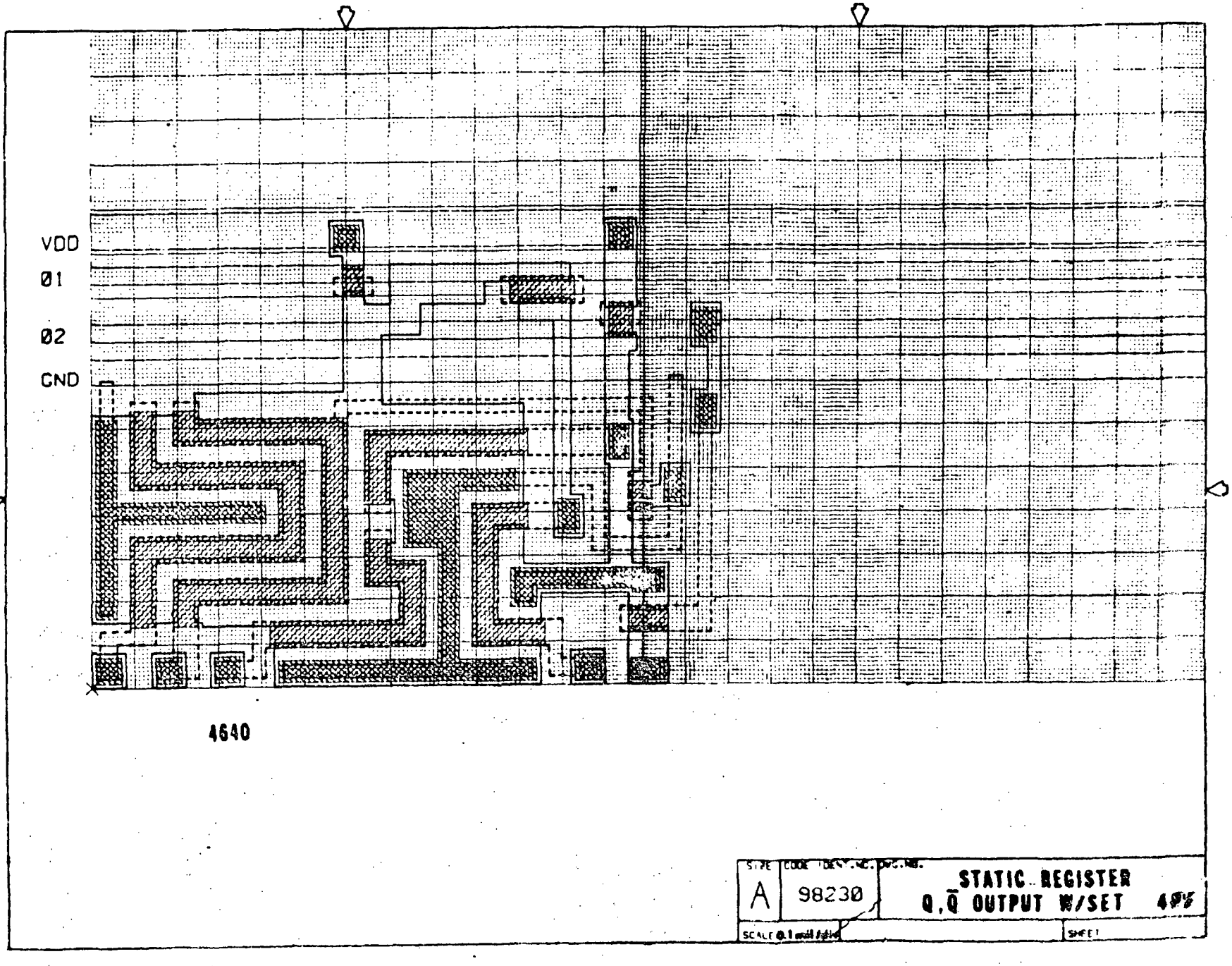
$$P = \overline{S_{t-1}} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

$$= [A_{t-1} \cdot B_{t-1} \cdot C_{t-1} + \overline{B_{t-1}} \cdot \overline{C_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_C	4	810
C_A	2	1500
C_B	3	1640
C_S	5	1750
C_P	6	980
PATTERN NO.		4640

STATIC REGISTER • 4640 • JUNE 1969
"0" AND "1" OUTPUTS WITH SET


VDD
Ø1
Ø2
GND
4640
SIZE
A
98230
STATIC REGISTER
Q,Q̄ OUTPUT W/SET
SHEET

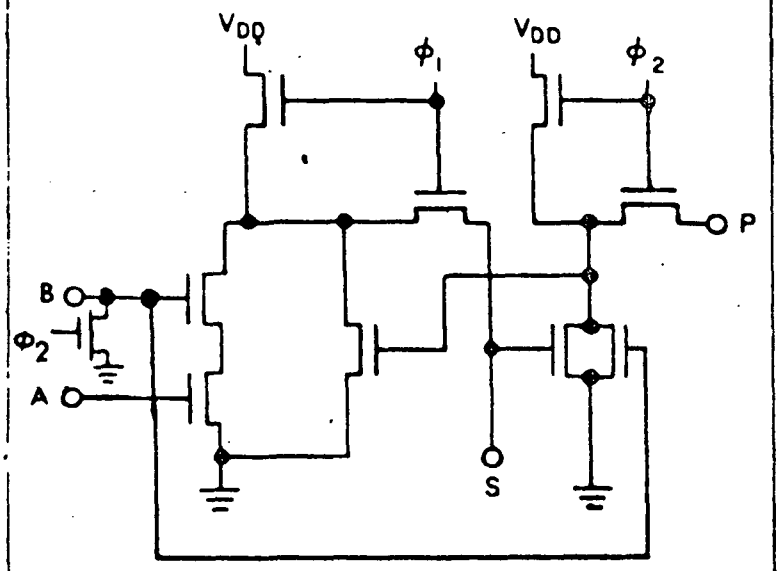
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"0" AND "1" OUTPUTS WITH KILL

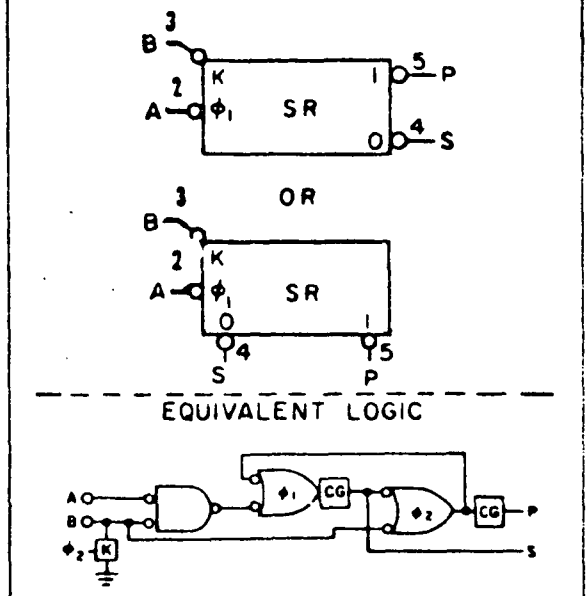
PATTERN NO. 4660 ($\phi_1\phi_2$)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE					
A	B	ϕ_1	S	ϕ_2	P
*	*	0	S_{t-1}	–	–
*	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
0	1	1	1	0	P_{t-1}
1	1	1	0	0	P_{t-1}
*	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
*	0	0	1	1	0
*	0	0	0	1	1
*MEANS EITHER STATE					

B IS THE SAMPLE INPUT

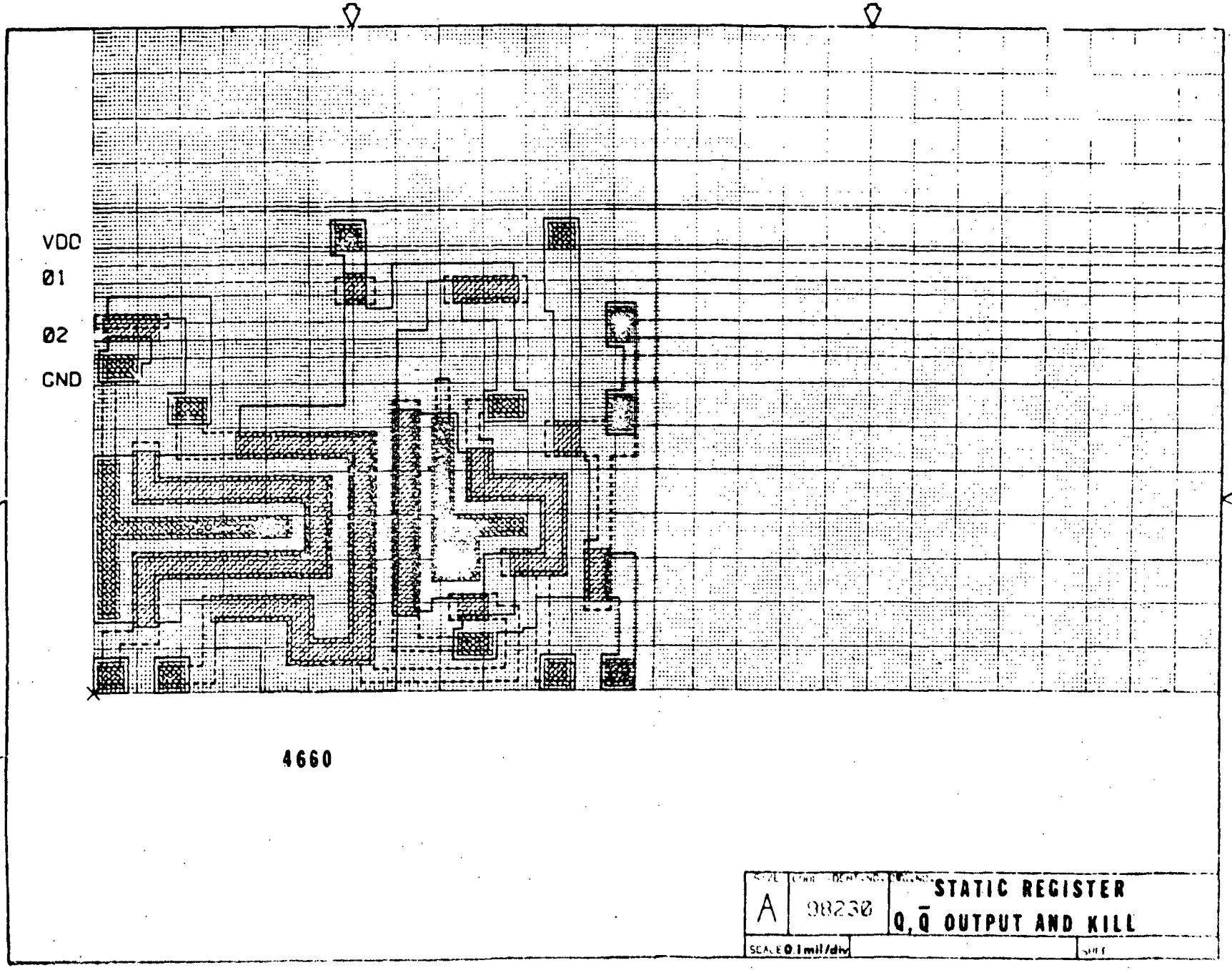
LOGIC EQUATIONS

$$S = [\bar{B} \cdot \overline{P_{t-1}} + \bar{A} \cdot B]\,\phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

$$P = \overline{S_{t-1}} \cdot \phi_2 + P_{t-1} \cdot \bar{\phi}_2$$

$$= [\overline{B_{t-1}} \cdot P_{t-1} + A_{t-1} \cdot B_{t-1}]\,\phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES		
CAPACITOR	PIN	CAPACITY IN fF
C_B	3	1860
C_A	2	1500
C_S	4	1570
C_P	5	840
PATTERN NO.		4660


VDD
Ø1
Ø2
GND
4660
A
98230
STATIC REGISTER
Q, Q̄ OUTPUT AND KILL
SCALE 0.1 mil/div

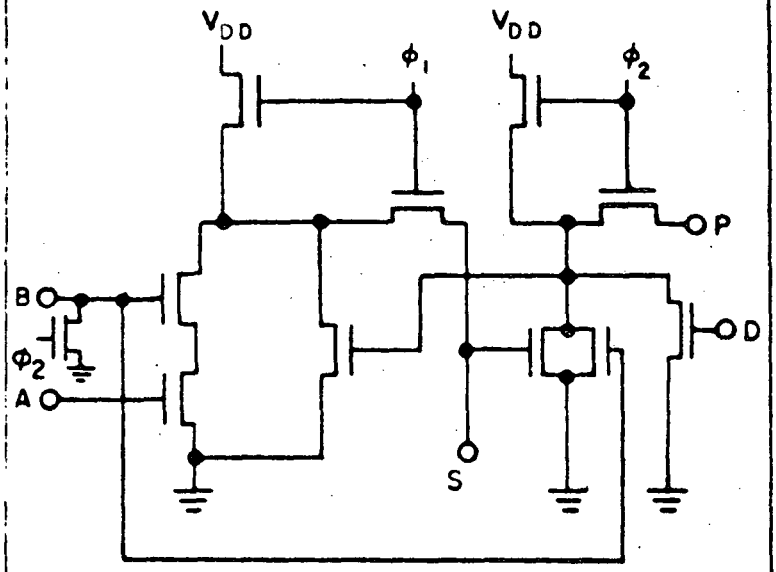
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"0" AND "1" OUTPUTS, RESET AND KILL

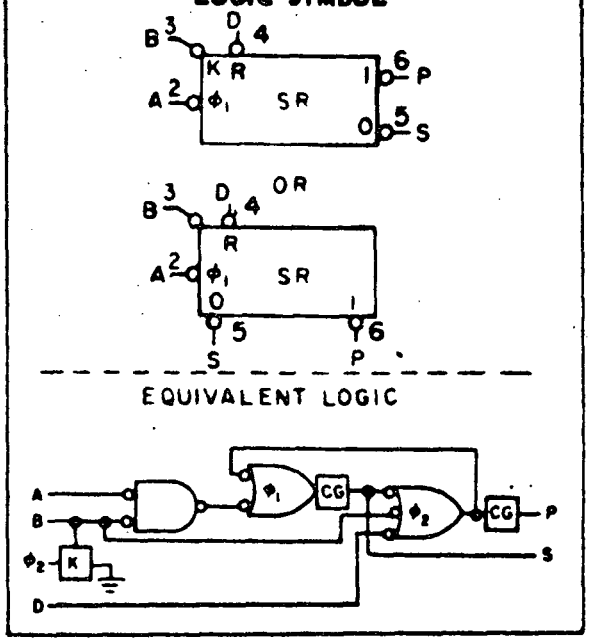
PATTERN NO. 4680 (ϕ_1, ϕ_2)

JUNE 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	D	ϕ_1	S	ϕ_2	P
·	·	*	0	S_{t-1}	–	–
·	0	0	1	$\overline{P_{t-1}}$	0	P_{t-1}
·	0	1	1	1	0	P_{t-1}
0	·	1	1	1	0	P_{t-1}
0	1	*	1	1	0	P_{t-1}
1	1	·	1	0	0	P_{t-1}
·	0	0	0	$\overline{P_{t-1}}$	1	P_{t-1}
·	0	1	0	*	1	0
·	0	0	0	1	1	0
·	0	0	0	0	1	1

*MEANS EITHER STATE

B IS THE SAMPLE INPUT

LOGIC EQUATIONS

$$S = [(\bar{A} + \bar{B}) \cdot D + B \cdot \bar{A} + \bar{B} \cdot \bar{D} \cdot \overline{P_{t-1}}] \cdot \phi_1 + S_{t-1} \cdot \bar{\phi}_1$$

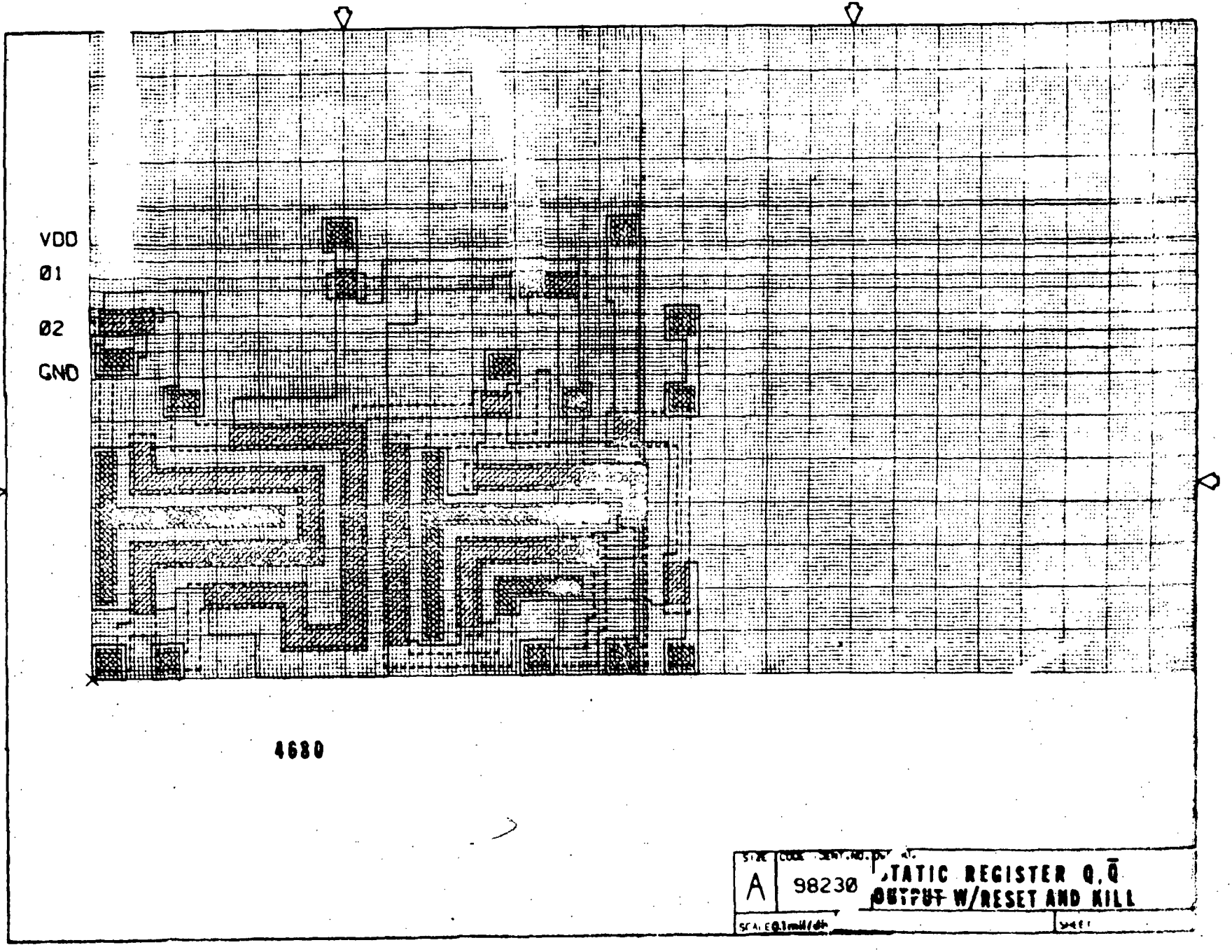
$$P = \overline{S_{t-1}} \cdot \bar{D} \cdot \phi_2 \cdot \bar{B} + P_{t-1} \cdot \bar{\phi}_2$$

$$= [A_{t-1} \cdot B_{t-1} + \overline{B_{t-1}} \cdot \overline{D_{t-1}} \cdot P_{t-1}] \cdot \phi_2 \cdot \bar{B} \cdot \bar{D} + P_{t-1} \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	1500
C_B	3	1840
C_S	5	1610
C_P	6	1020
C_D	4	660
PATTERN NO.		4680

STATIC REGISTER • 4pF • 4680 • JUNE 1969
"0" AND "1" OUTPUTS, RESET AND KILL


VDD
Ø1
Ø2
GND
4680
A
98230
STATIC REGISTER Q,Q̄
OUTPUT W/RESET AND KILL

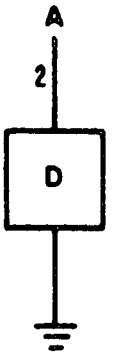
BANNING THICK OXIDE STANDARD CELL

PROTECTIVE DIODE PATTERN NO. 5020

JANUARY 1969

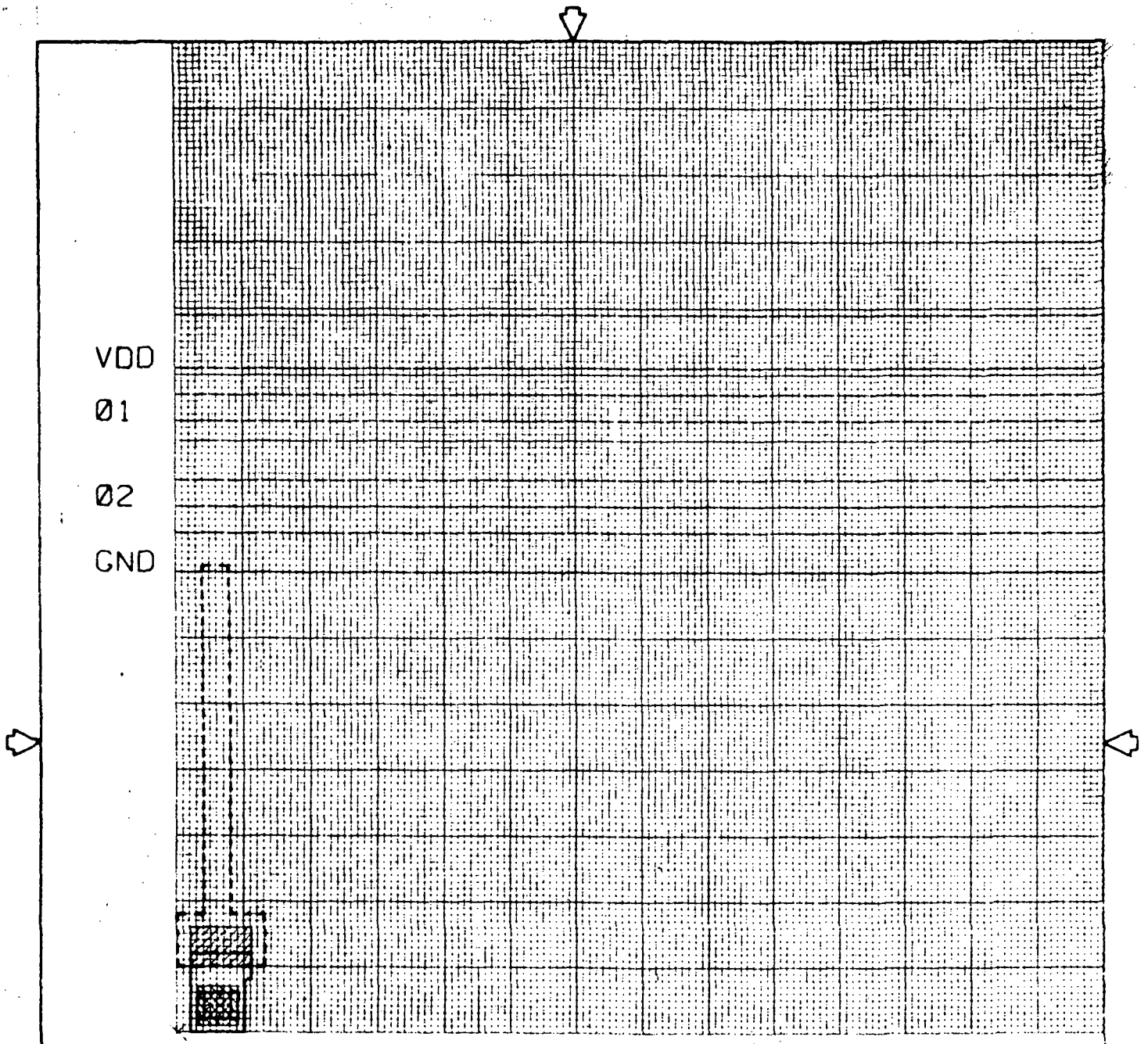
SCHEMATIC

LOGIC SYMBOL



CELL I/O CAPACITIES		
CAPACITOR	PIN	CAPACITY IN fF
C_A	2	95
PATTERN NO.		5020

PROTECTIVE DIODE · 5020 · JANUARY 1969



5020

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	PROTECTIVE DIODE
SCALE		SHEET

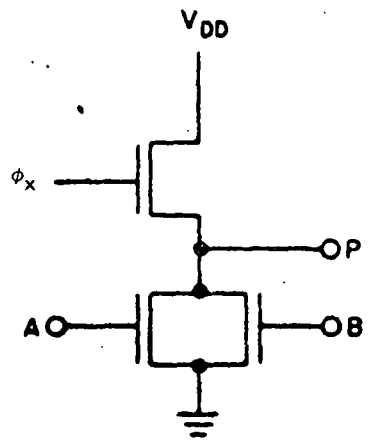
BANNING THICK OXIDE STANDARD CELL

TWO INPUT NOR, 9pt

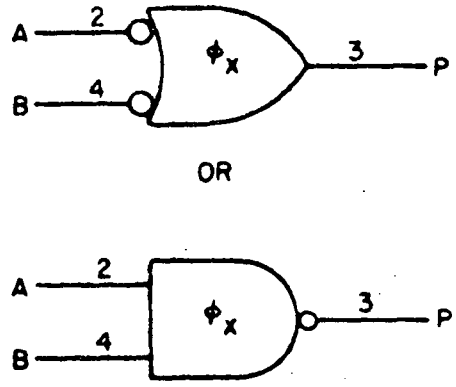
PATTERN NO. 5030 (ϕ_1)
5040 (ϕ_2)

JANUARY 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	ϕ_x	P
0	0	0	P_{t-1}
1	*	*	0
*	1	*	0
0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

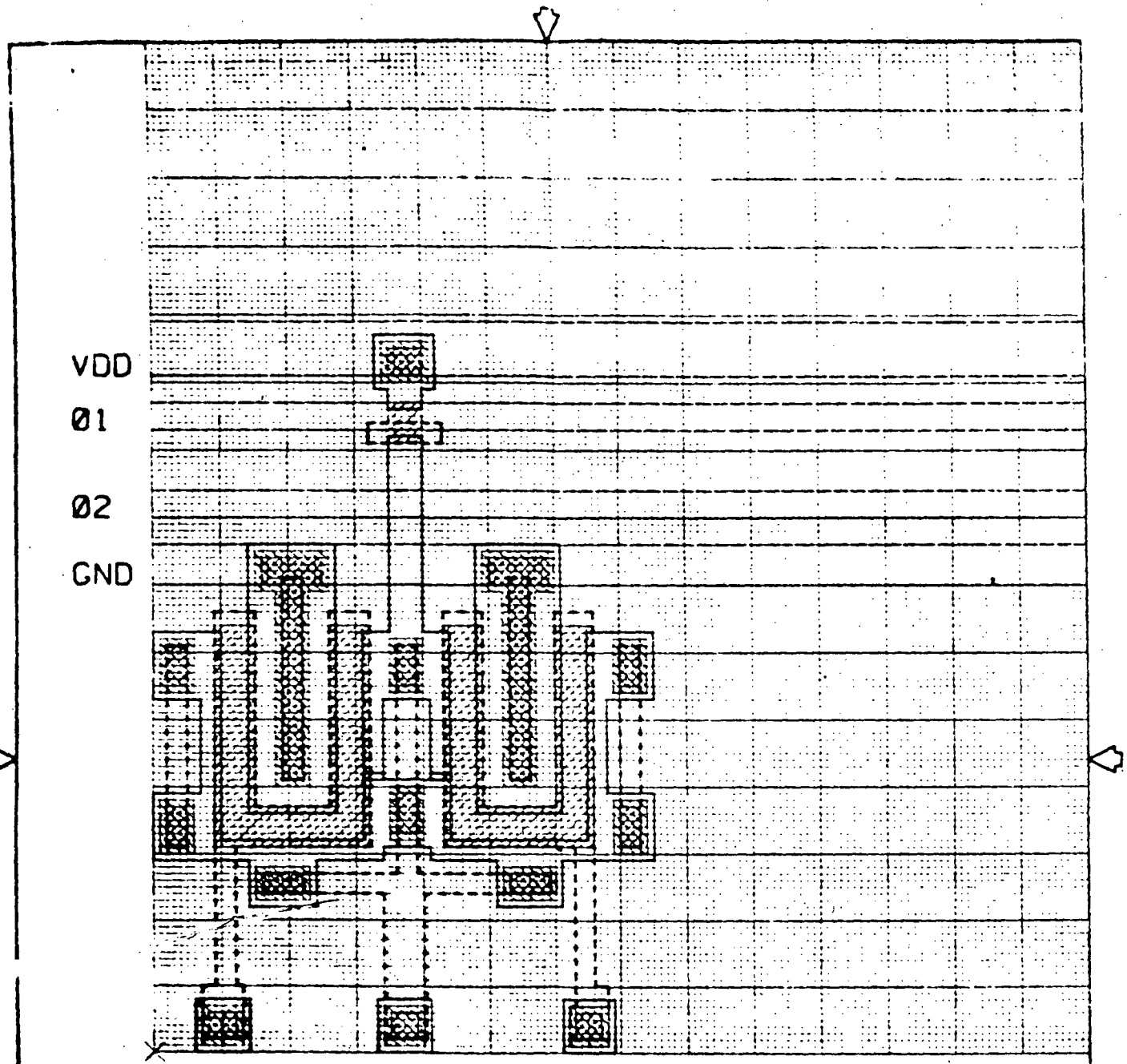
$$P = \overline{(A + B)} \cdot \overline{\phi_x} \cdot P_{t-1} + \overline{(A + B)} \cdot \phi_x$$

$$= \bar{A} \cdot \bar{B} \cdot \overline{\phi_x} \cdot P_{t-1} + \bar{A} \cdot \bar{B} \cdot \phi_x$$

CELL I/O CAPACITIES

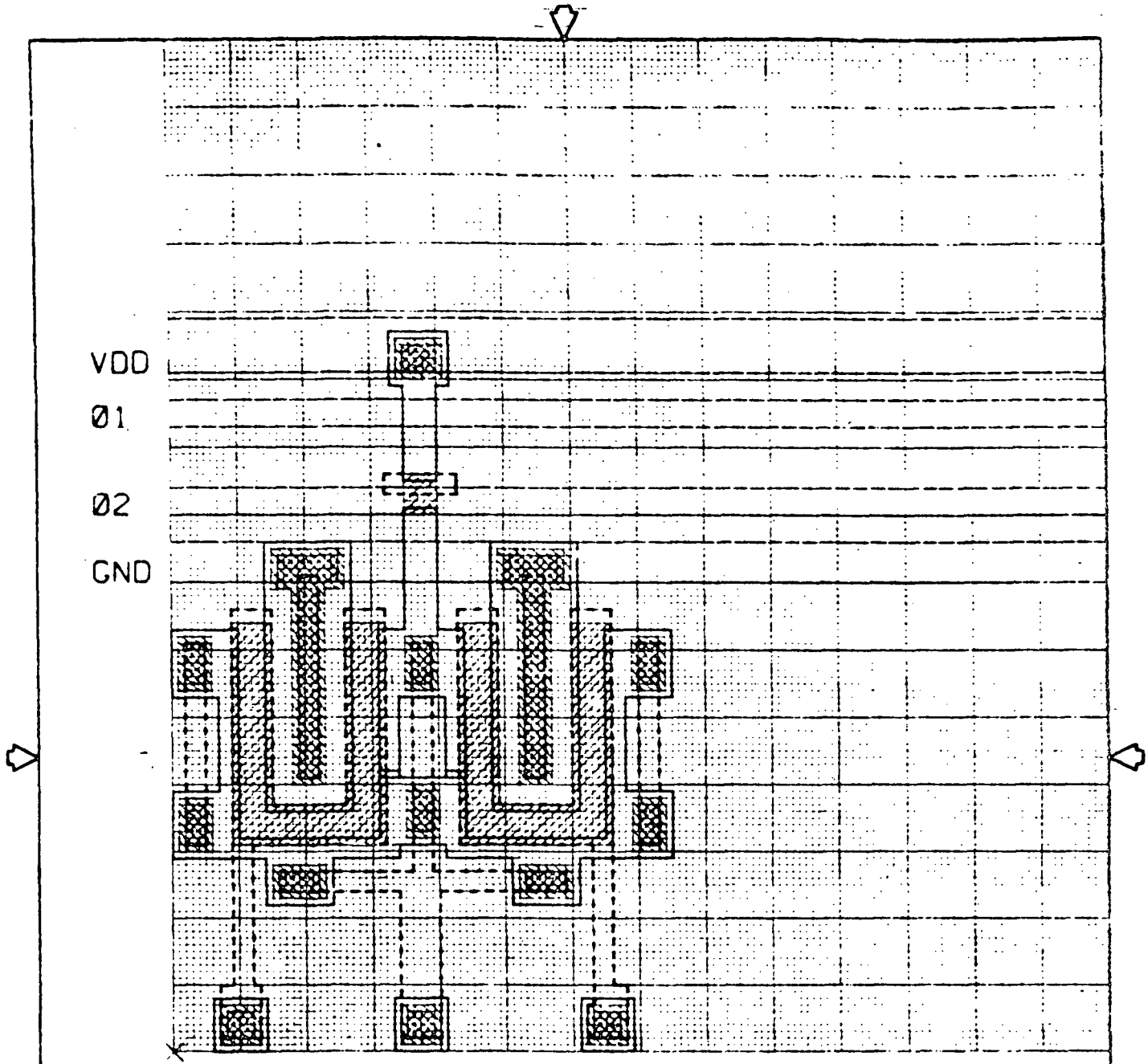
CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	990	990
C_P	3	910	910
C_B	4	990	990
PATTERN NO.		5030	5040

TWO INPUT NOR · 5030/5040 · JANUARY 1969



5030

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	2 INPUT NOR, 9PF
SCALE		SHEET



5040

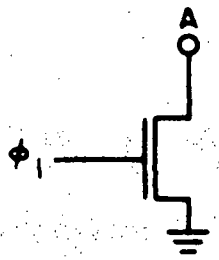
SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	2 INPUT NOR, 9 PF	
SCALE			SHEET

BANNING THICK OXIDE STANDARD CELL

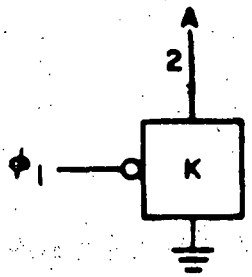
KILLER, ϕ_1 CONTROLLED — **PATTERN NO. 5090 (ϕ_1)**

JANUARY 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

ϕ_1	A
0	A
1	0

*MEANS EITHER STATE

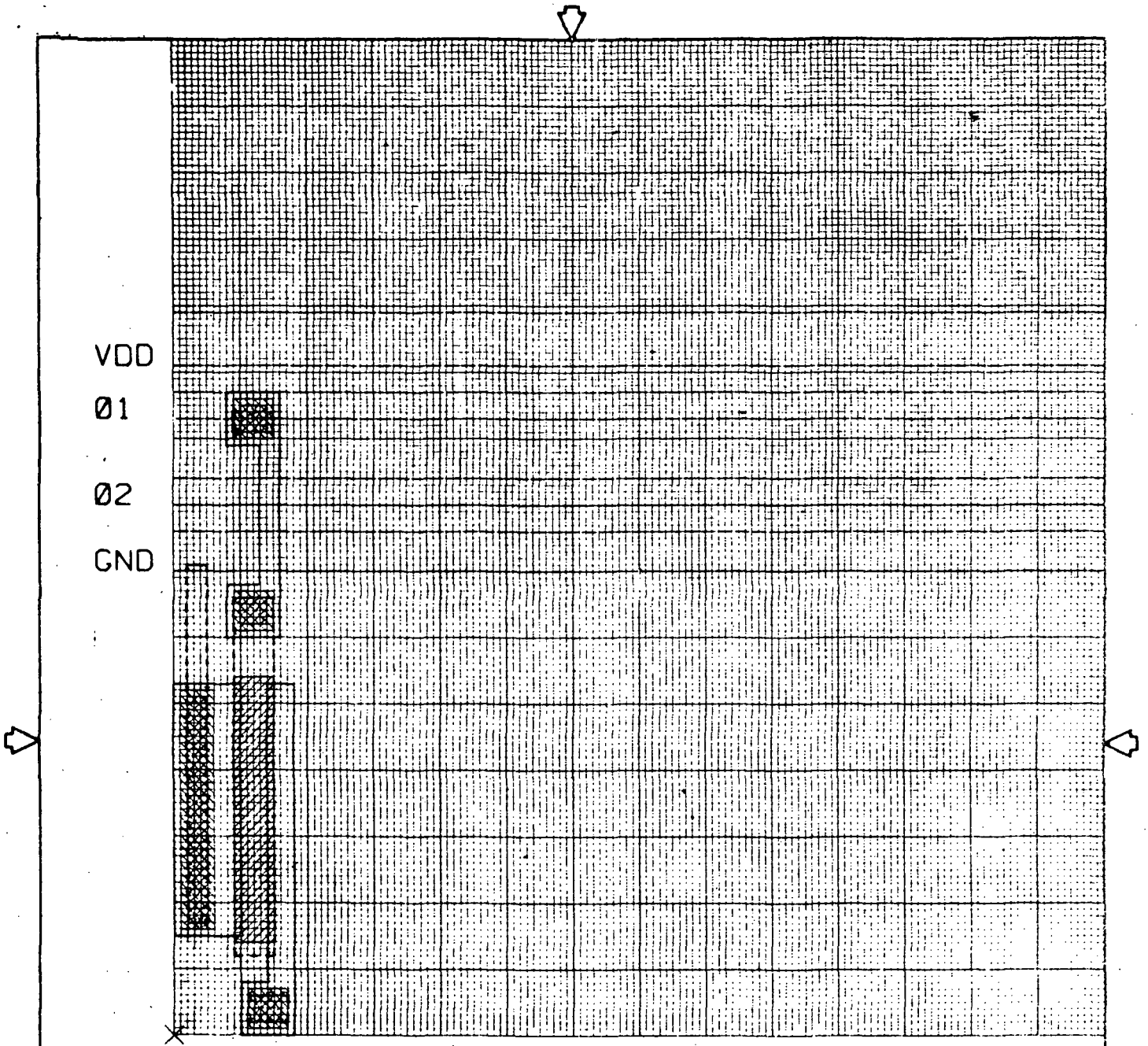
LOGIC EQUATIONS

$$A = A \cdot \bar{\phi}_1$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	170
PATTERN NO.		6040

KILLER, ϕ_1 CONTROLLED · 5090 · JANUARY 1969



5090

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	KILLER Ø1
SCALE		SHEET

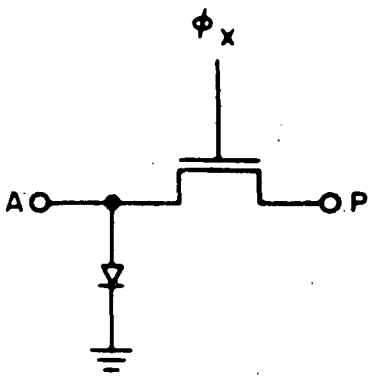
BANNING THICK OXIDE STANDARD CELL

PROTECTED CLOCK GATE

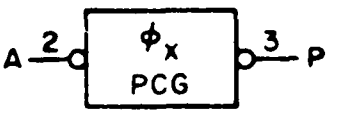
PATTERN NO. 6000 (ϕ_2)
6010 (ϕ_1)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_x	P
*	0	P_{t-1}
0	1	0
1	1	1

*MEANS EITHER STATE

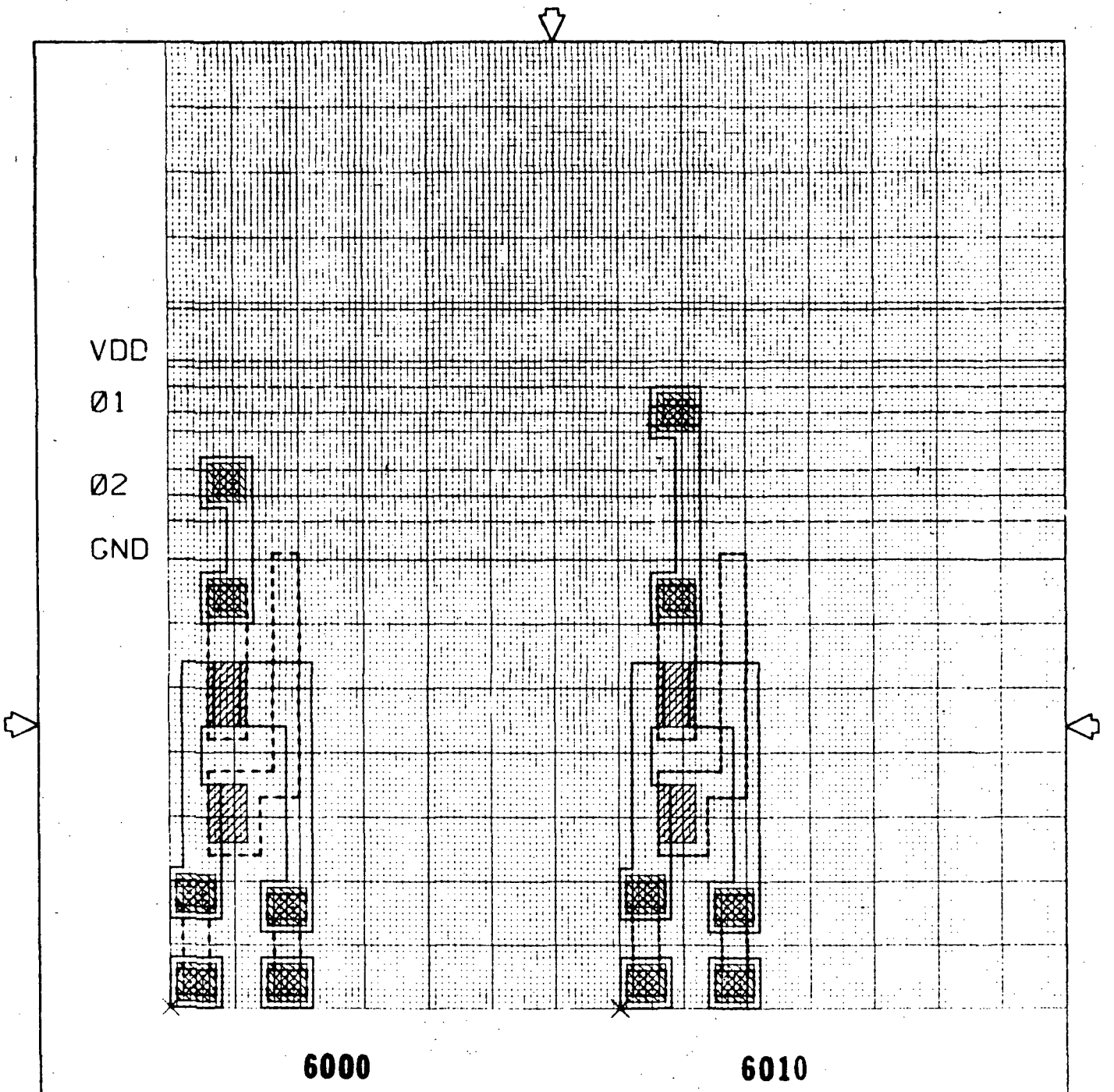
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \overline{\phi}_x + A \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	210	210
C_P	3	240	240
PATTERN NO.		6000	6010

PROTECTED CLOCK GATE • 6000 6010 • APRIL 1968



SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	**PROTECTED CLOCK GATE**
SCALE **0.1mil/div**		SHEET

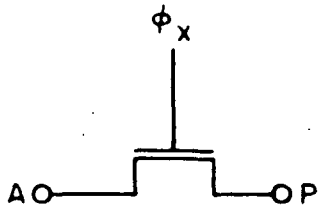
BANNING THICK OXIDE STANDARD CELL

CLOCK GATE

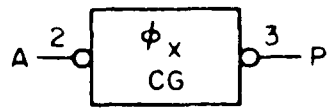
PATTERN NO. 6020 (ϕ_2)
6030 (ϕ_1)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_x	P
	0	P_{t-1}
0	1	0
1	1	1

*MEANS EITHER STATE

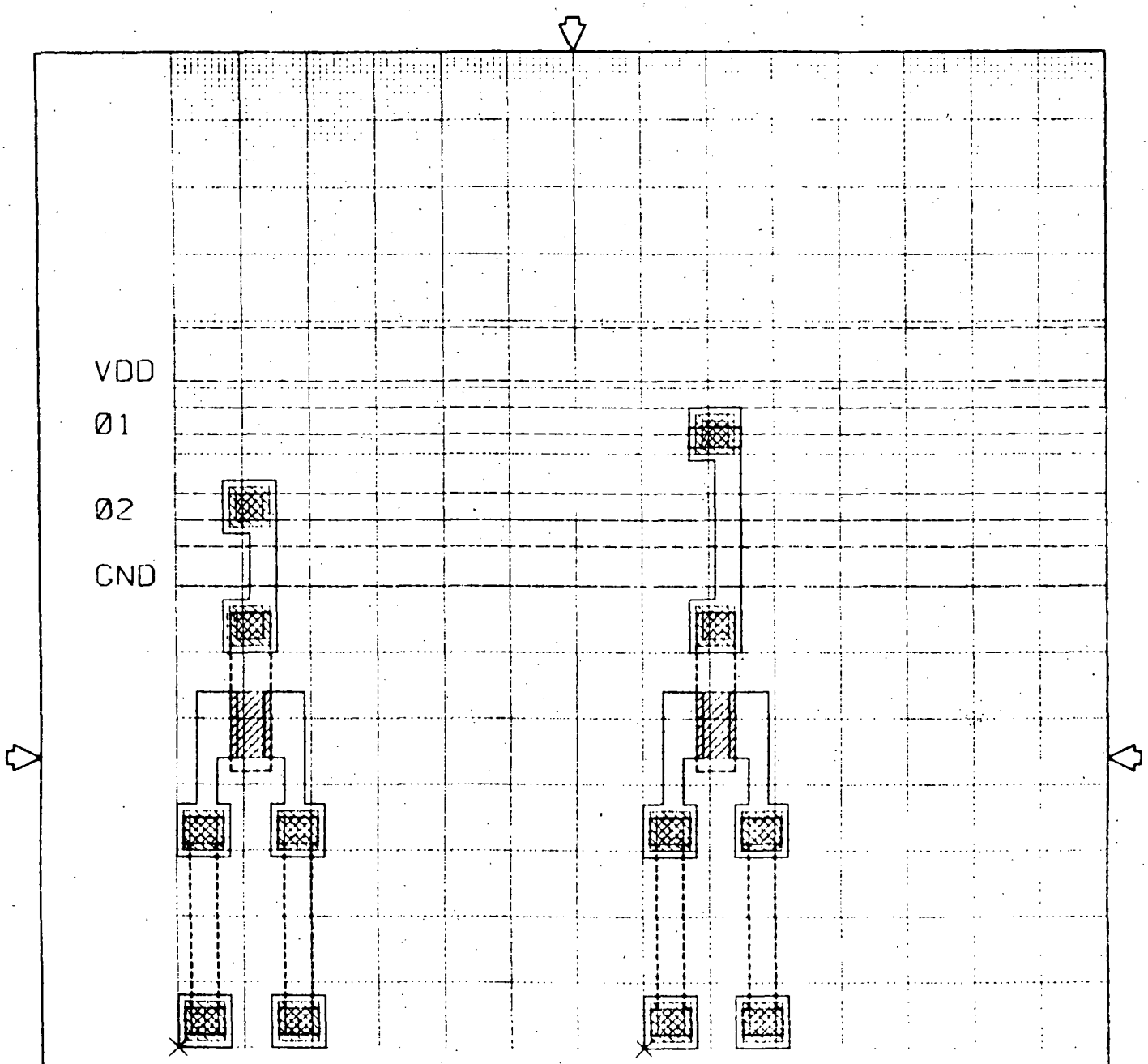
LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{\phi}_x \cdot A \cdot \phi_x$$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	170	170
C_P	3	170	170
PATTERN NO.		6020	6030

CLOCK GATE • 6020 6030 • APRIL 1968



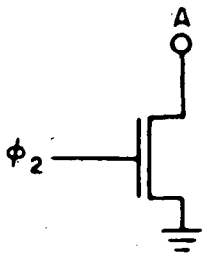
SIZE	CODE IDENT. NO.	DWG. NO.
A	98230	CLOCK GATE
SCALE 0.1 mil/div		SHEET

BANNING THICK OXIDE STANDARD CELL

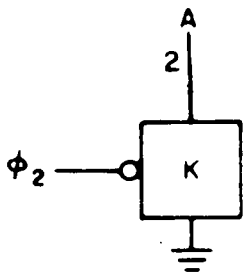
KILLER, ϕ_2 CONTROLLED · **PATTERN NO. 6040 (ϕ_2)**

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

ϕ_2	A
0	A
1	0

*MEANS EITHER STATE

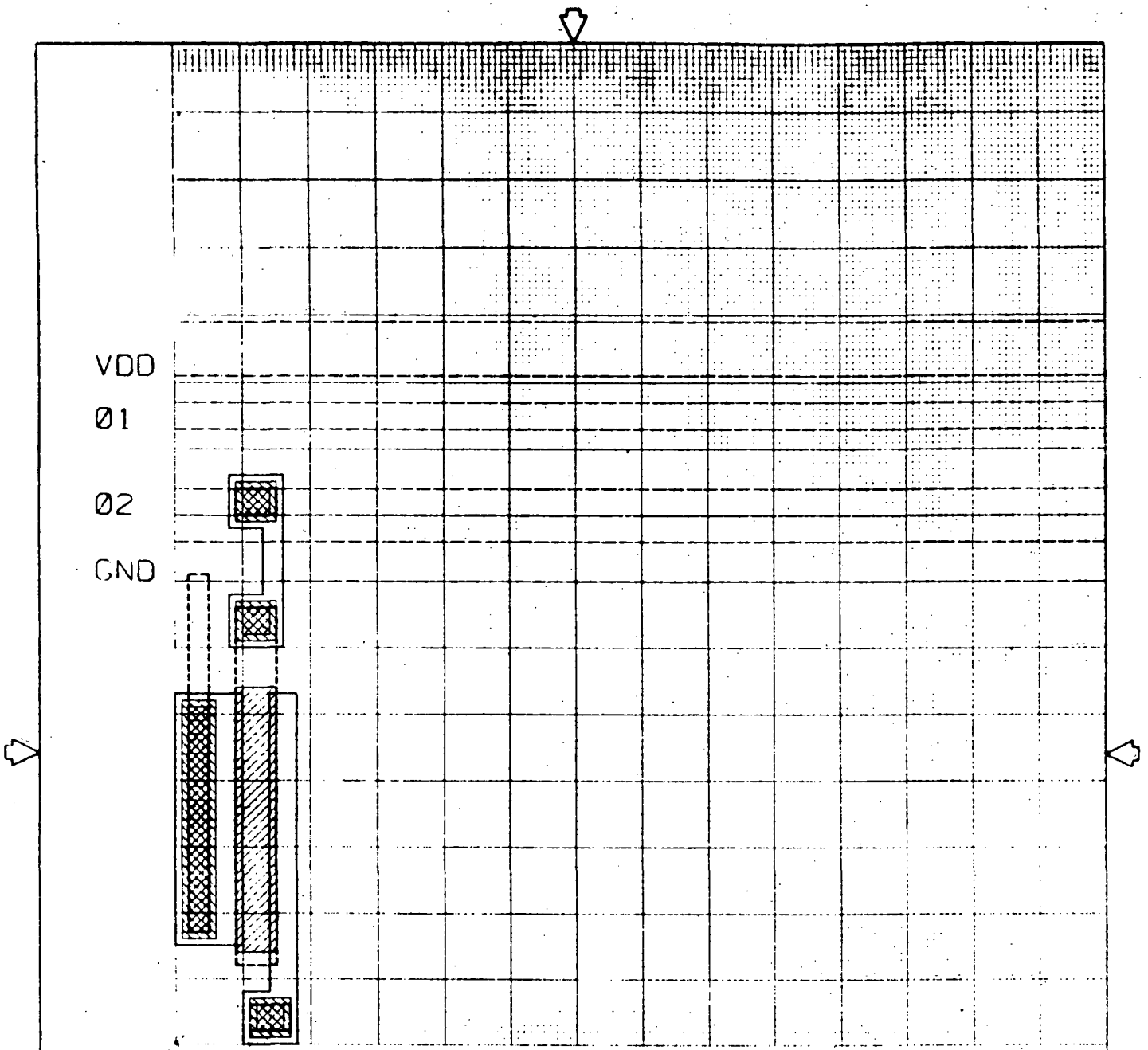
LOGIC EQUATIONS

$$A - A \cdot \bar{\phi}_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	170
PATTERN NO.		6040

KILLER, ϕ_2 CONTROLLED • 6040 • APRIL 1968



6040

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	KILLER Ø2
SCALE		SHEET

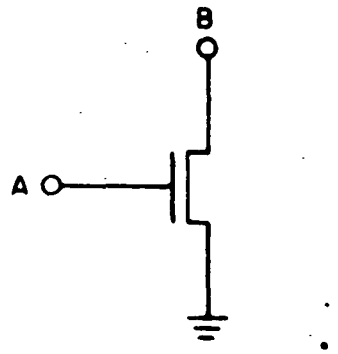
BANNING THICK OXIDE STANDARD CELL

KILLER, SIGNAL CONTROLLED

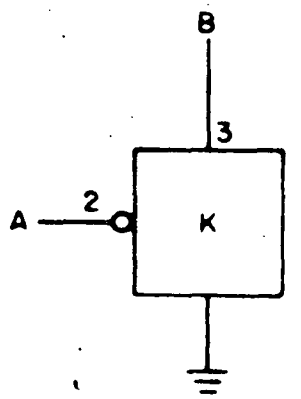
PATTERN NO. 6050

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B
0	B
1	0

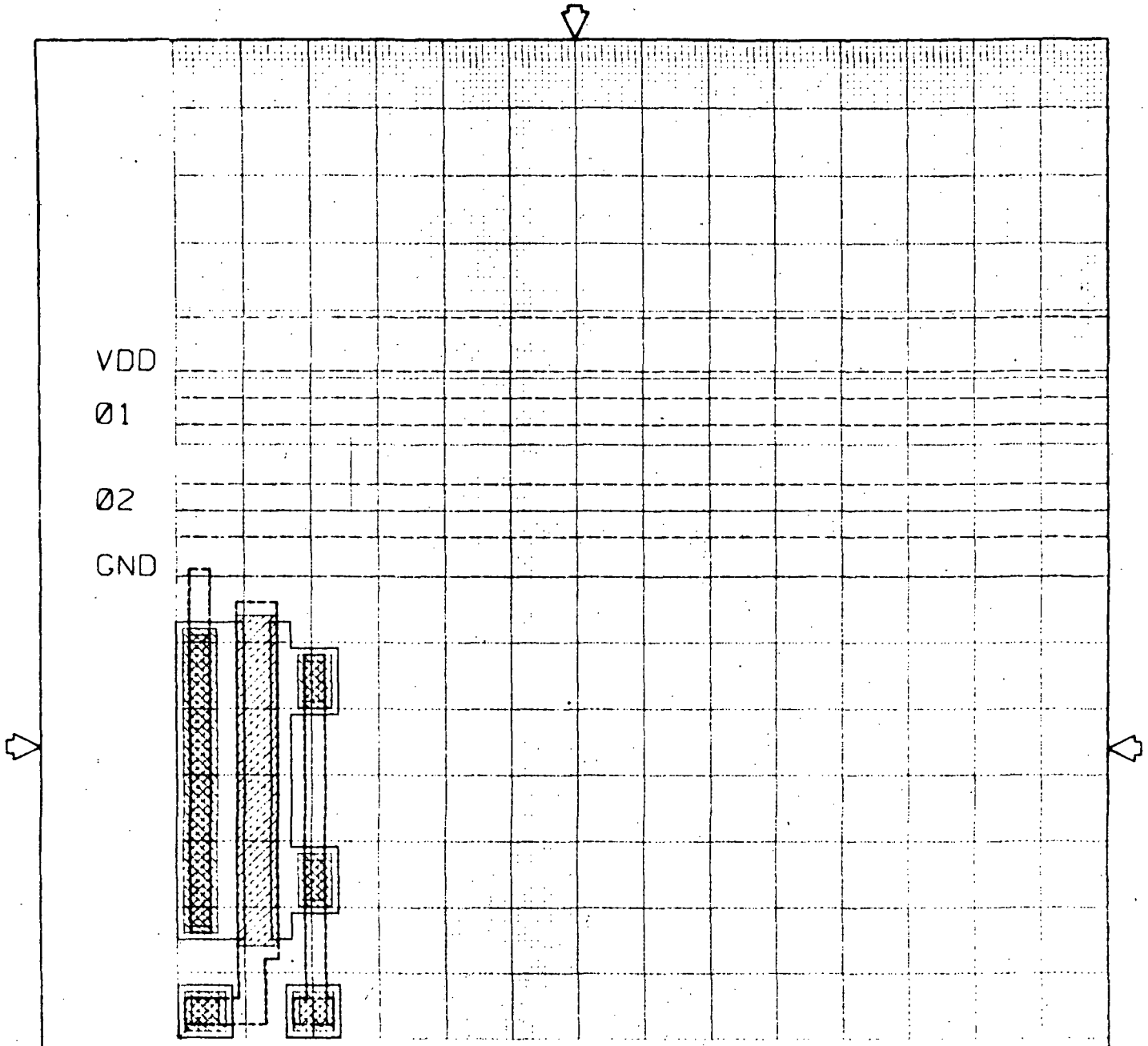
*MEANS EITHER STATE

LOGIC EQUATIONS

$$B = B \cdot \bar{A}$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	460
C_P	3	270
PATTERN NO.		6050



6050

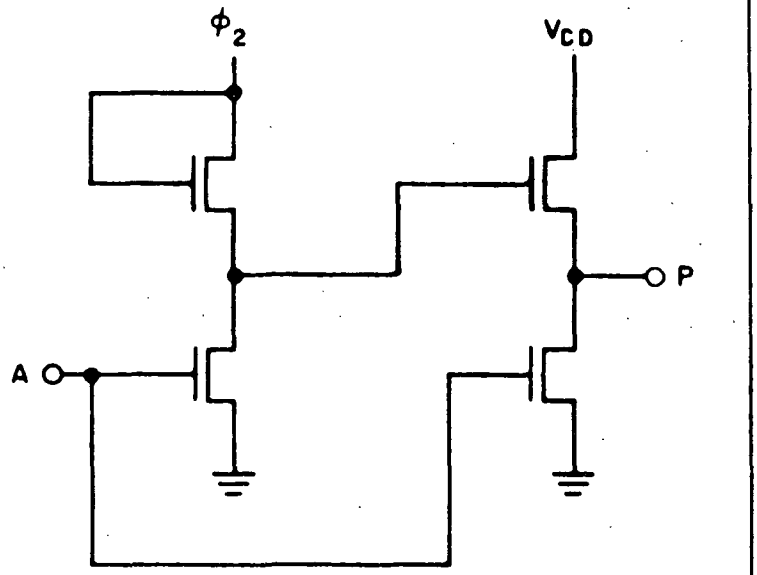
SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	**KILLER (SIGNAL INPUT)**
SCALE **0.1mil/div**		SHEET

BANNING THICK OXIDE STANDARD CELL

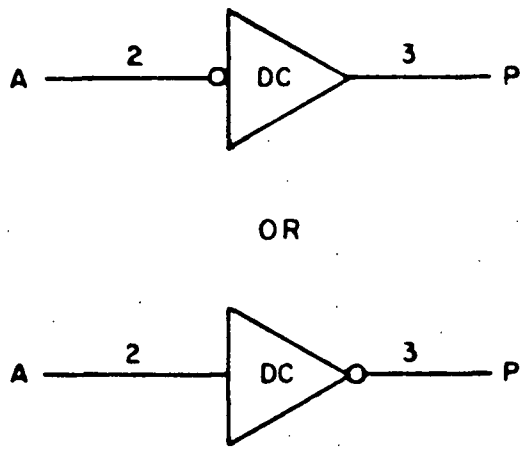
D. C. BUFFER, 25pF — **PATTERN NO. 6060 (ϕ_2)**

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_2	P
0	0	P_{t-1}
1	0	0
1	1	0
0	1	1

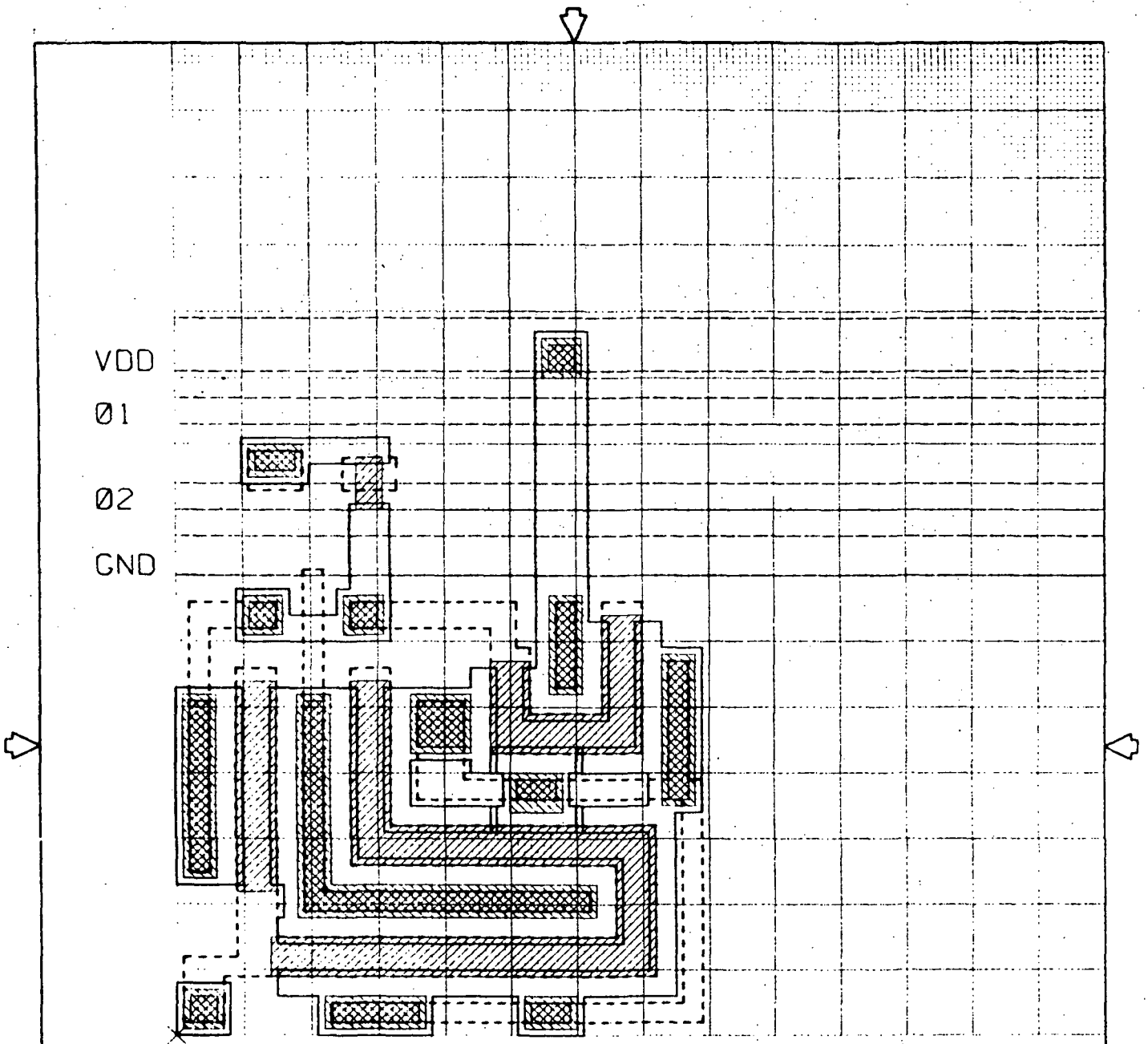
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{A} \cdot \bar{\phi}_2 + \bar{A} \cdot \phi_2$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	2110
C_P	3	960
PATTERN NO.		6060



6060

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	**DC BUFFER (28 PF)**
SCALE **0.1mil/div**		SHEET

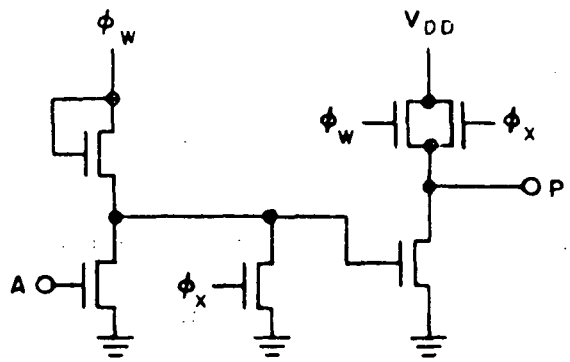
BANNING THICK OXIDE STANDARD CELL

PRECHARGE BUFFER, 53pF

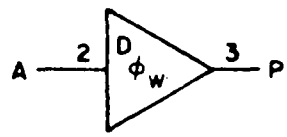
PATTERN NO. 6070 (ϕ_1) 6080 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_W	ϕ_X	P
0	1	0	0
*	0	1	1
1	1	0	1

*MEANS EITHER STATE

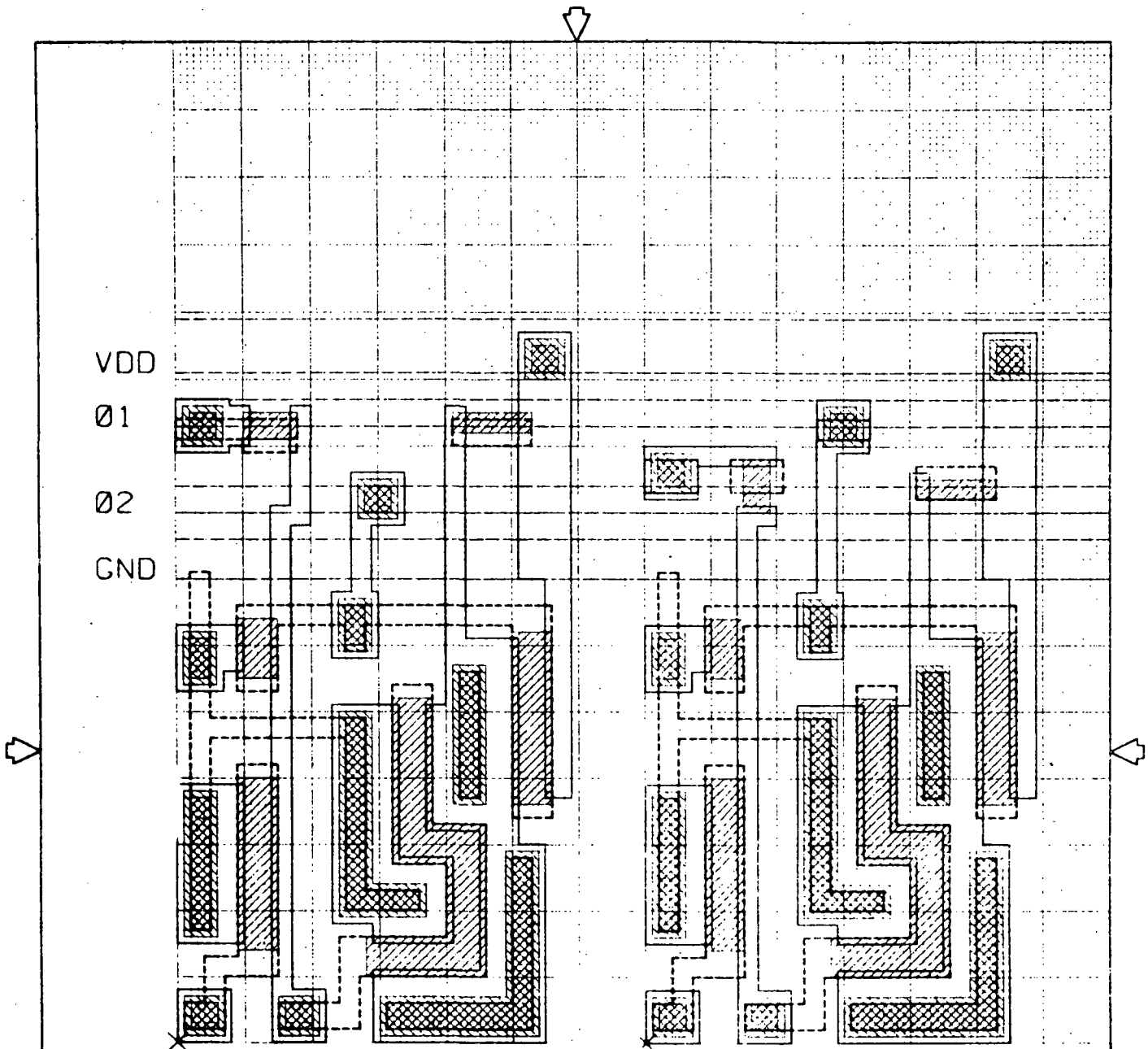
LOGIC EQUATIONS

$P = A \cdot \phi_W + \phi_X$

CELL I O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	370	370
C_P	3	680	660
PATTERN NO.		6070	6080

53pF PRECHARGE BUFFER • 6070 6080 • APRIL 1968



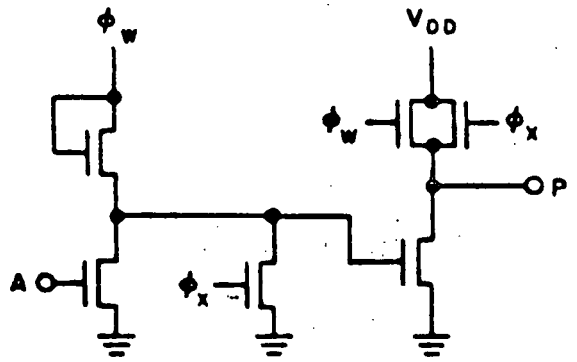
SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		PRECHARGED BUFFER (53PF)
SCALE 0.1mil/div			SHEET

BANNING THICK OXIDE STANDARD CELL

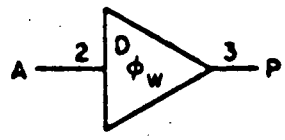
PRECHARGE BUFFER, 78pF — **PATTERN NO.** 6090 (ϕ_1) 6100 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_w	ϕ_x	P
0	1	0	0
*	0	1	1
1	1	0	1

*MEANS EITHER STATE

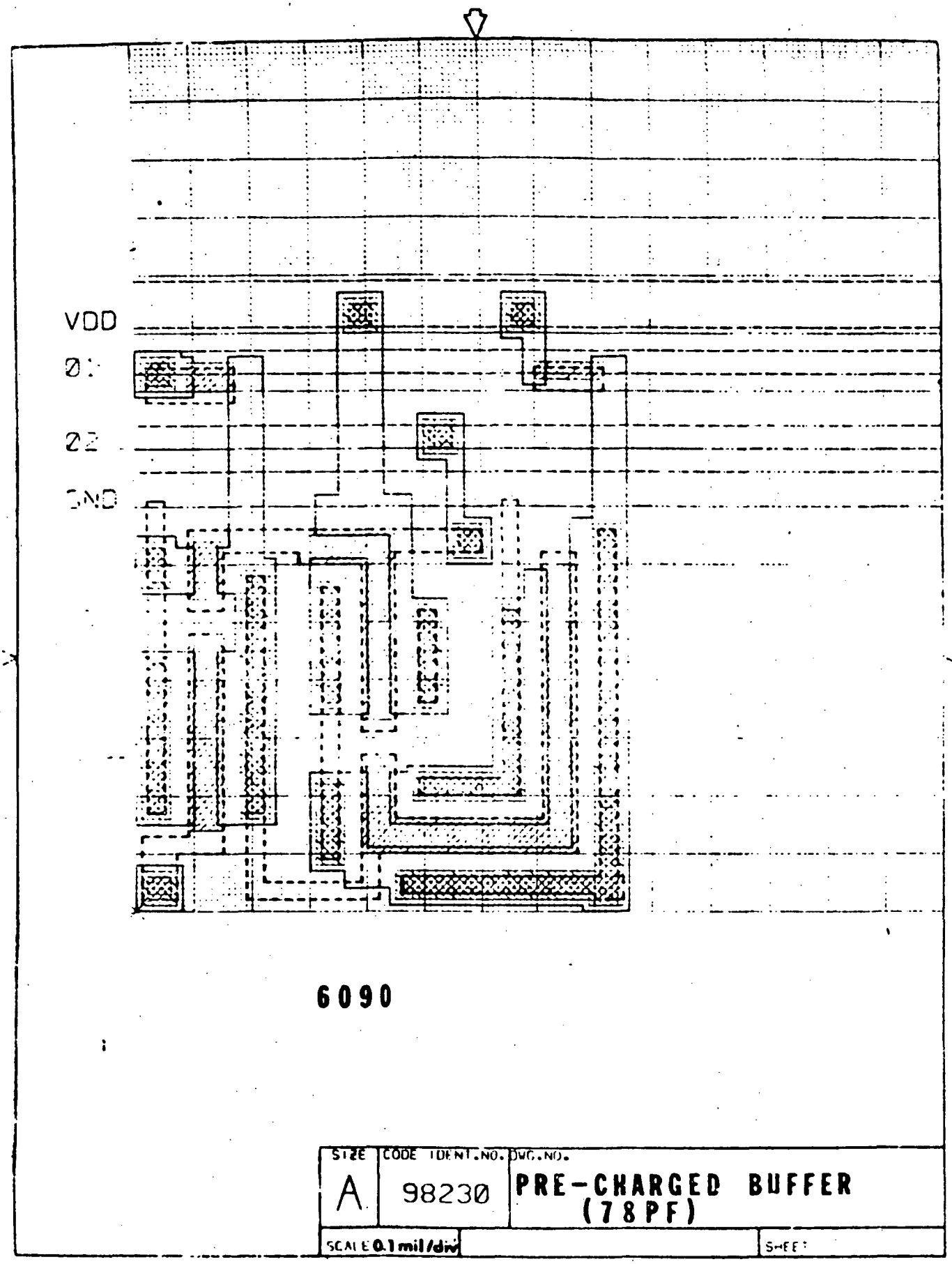
LOGIC EQUATIONS

$$P = A \cdot \phi_w + \phi_x$$

CELL I/O CAPACITIES

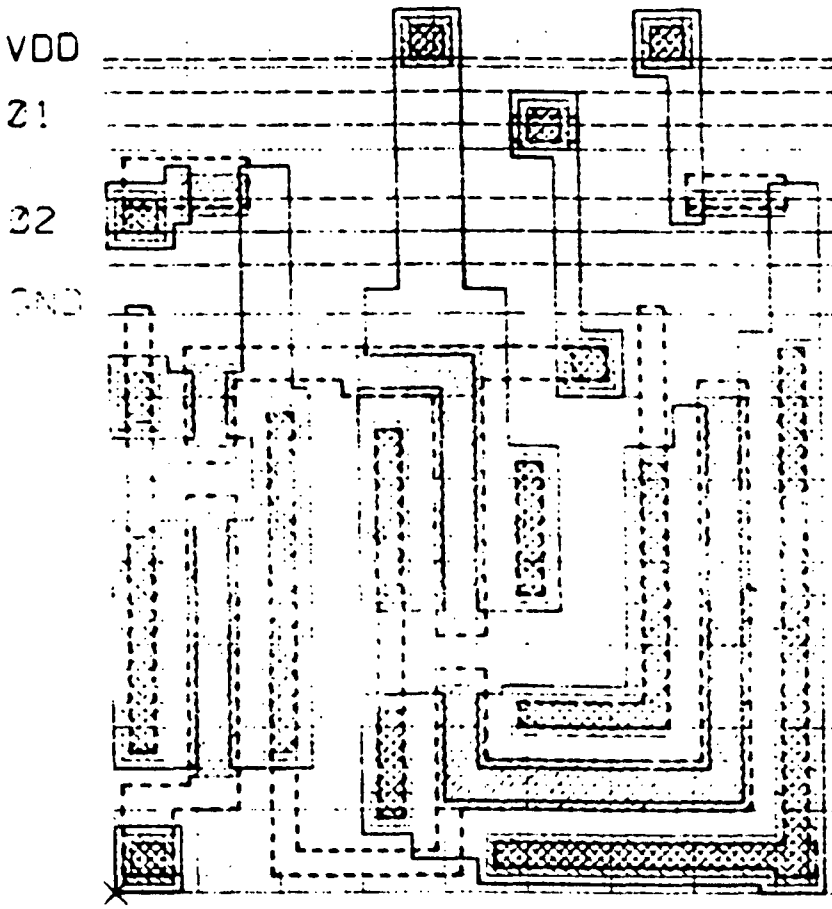
CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	440	440
C_P	3	960	920
PATTERN NO.		6090	6100

78pF PRECHARGE BUFFER • 6090/6100 • APRIL 1968



6090

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	PRE-CHARGED BUFFER (78PF)	
SCALE 0.1 mil/div			SHEET



6100

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	PRE-CHARGED BUFFER (78PF)	
SCALE 0.1mil/div			SHEET

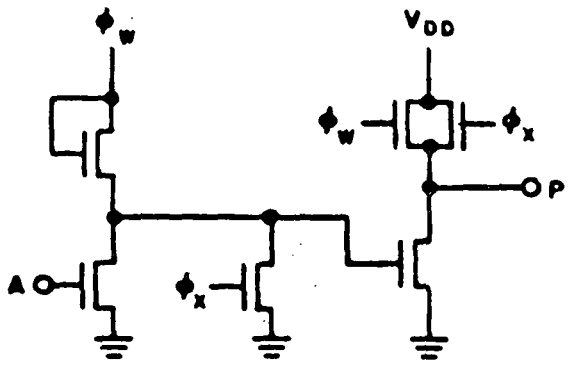
BANNING THICK OXIDE STANDARD CELL

PRECHARGE BUFFER, 103pF

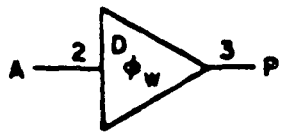
PATTERN NO. 6110 (ϕ_1) 6120 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_w	ϕ_x	P
0	1	0	0
*	0	1	1
1	1	0	1

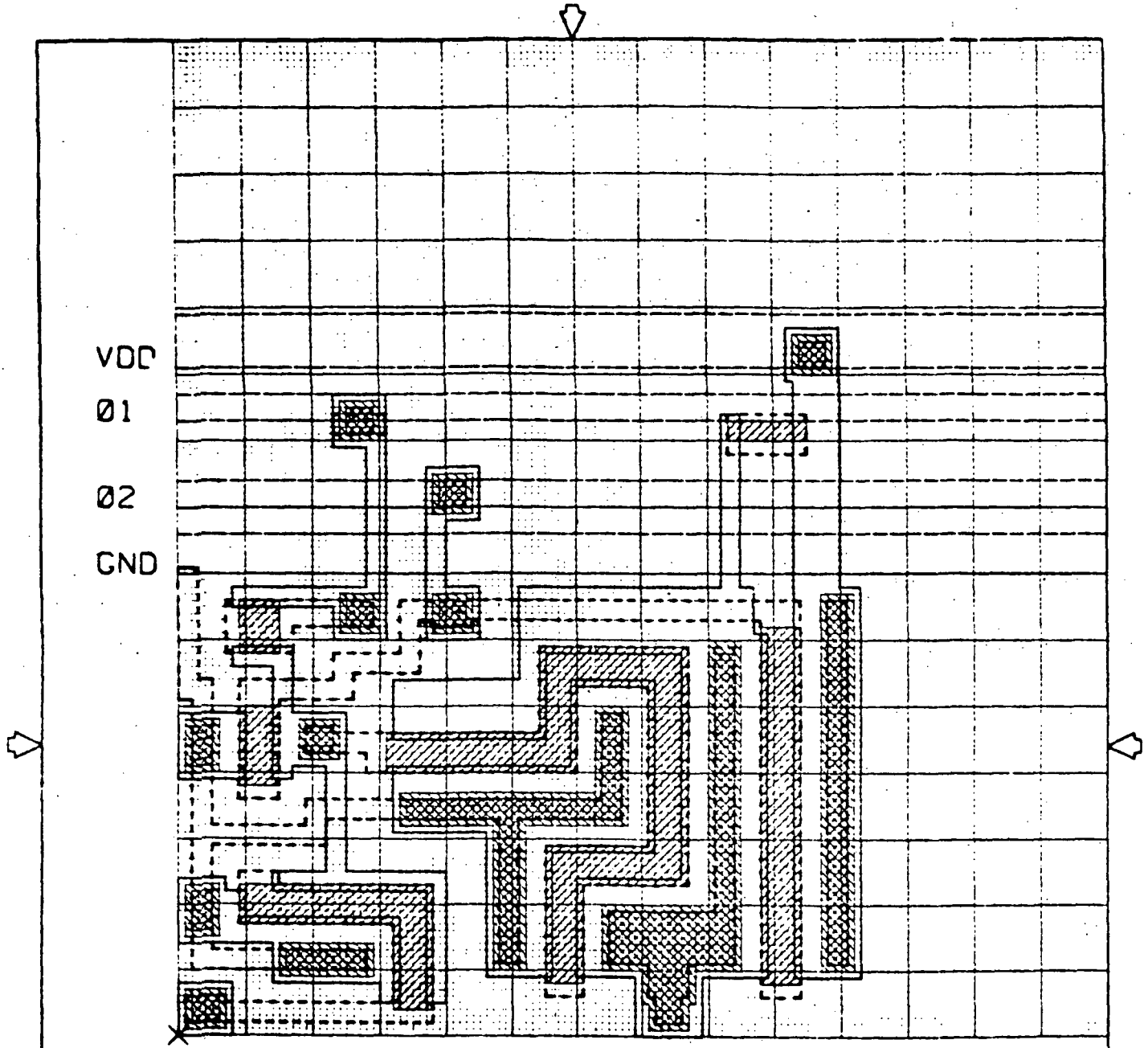
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = A \cdot \phi_w + \phi_x$$

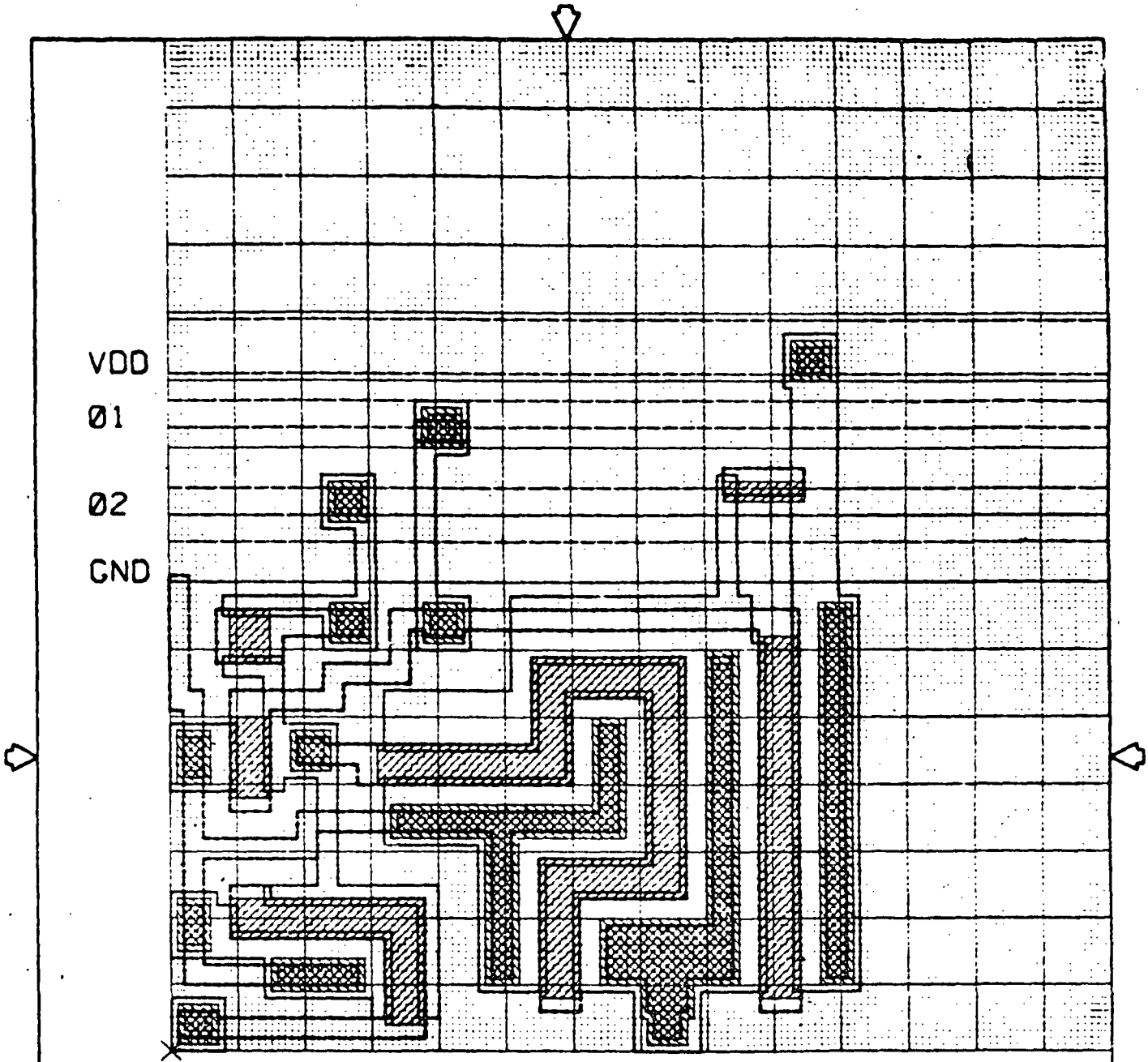
CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	580	570
C_P	3	1140	1130
PATTERN NO.		6110	6120



6110

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	PRE-CHARGED BUFFER (103PF)
SCALE 0.1mil/div		SHEET



6120

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	PRECHARGED BUFFER (103Pf)
SCALE@.1mil/div		SHEET

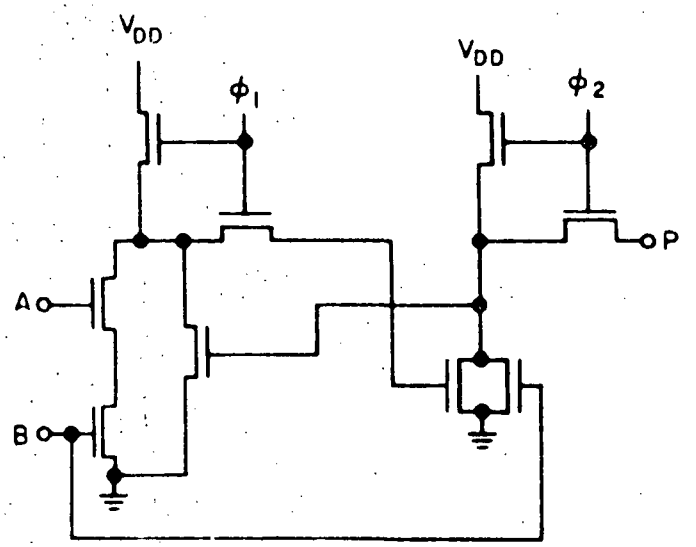
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER STRING START

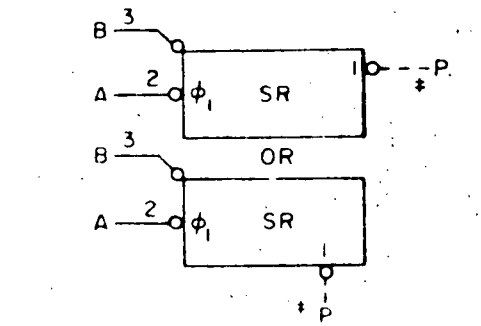
PATTERN NO. 6140 (ϕ_1 ϕ_2)

APRIL 1968

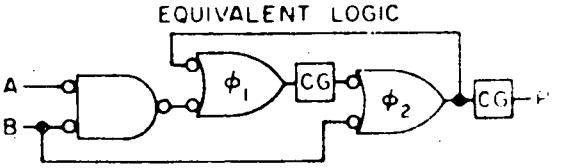
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

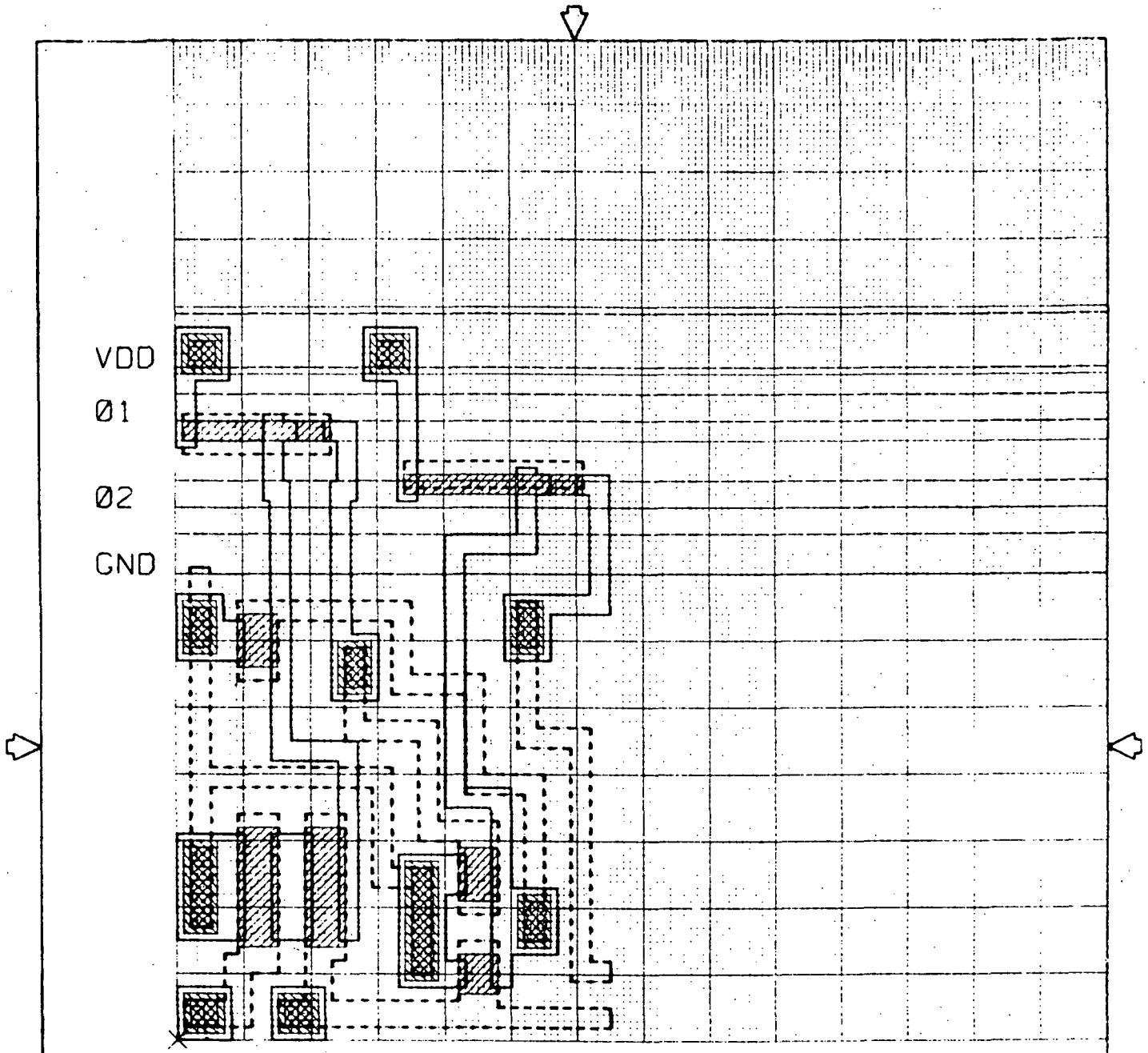
LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B}\,[A_{t-1}\,B_{t-1} + \overline{B_{t-1}}\,P_{t-1}]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	280
C_B	3	380
PATTERN NO.		6140

‡ P IS AN INTERNAL OUTPUT CONNECTION TO A 6160 OR 6180 CELL INPUT
THE B INPUT IS ALSO INTERNALLY CONNECTED TO B OF 6160 OR 6180 CELLS



6140

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	STATIC REGISTER STRING START
SCALE 0.1mil/div		SHEET

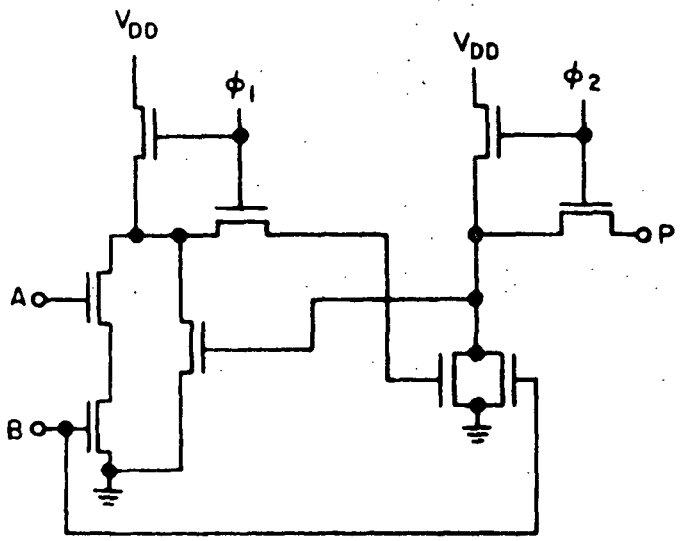
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER STRING MIDDLE

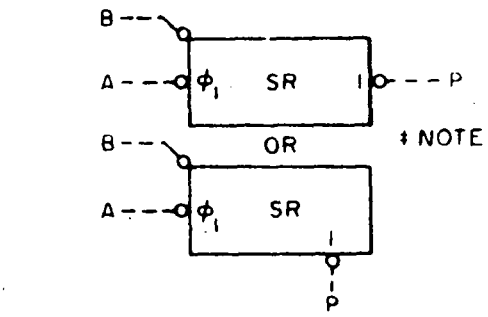
PATTERN NO. 6160 [ϕ_1 ϕ_2]

APRIL 1968

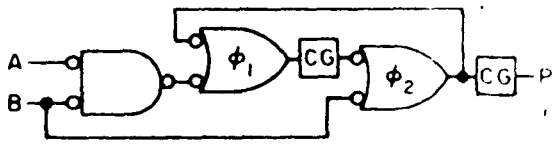
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

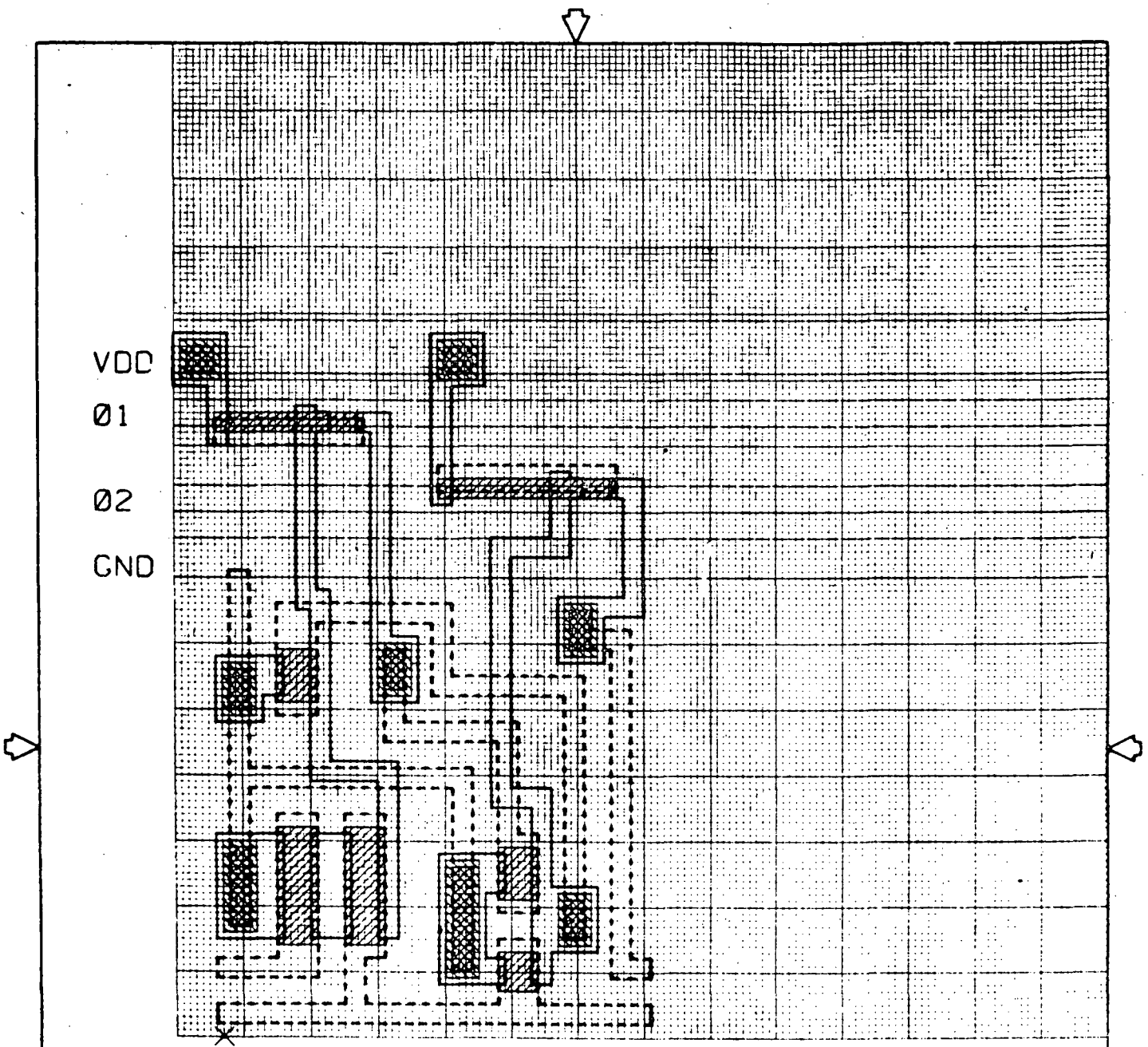
LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B} \left[A_{t-1} B_{t-1} + \overline{B_{t-1}} P_{t-1} \right]$$

CELL I/O CAPACITIES (NONE)

CAPACITOR	PIN	CAPACITY IN fF	
PATTERN NO.			

‡A AND B ARE INTERNAL INPUT CONNECTIONS FROM A 6140 OR 6160 CELL
P IS AN INTERNAL OUTPUT CONNECTION TO A 6160 OR 6180 CELL INPUT



6160

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	STATIC REGISTER STRING MIDDLE
SCALE 0.1mil/div		SHEET

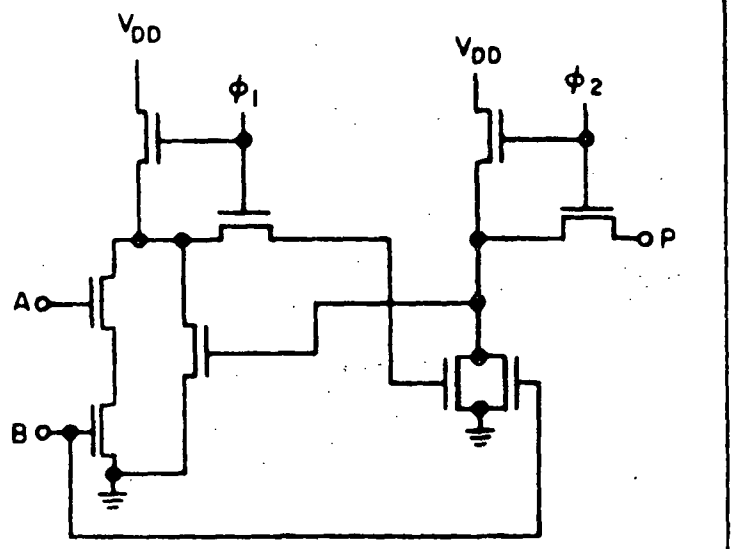
BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER STRING END

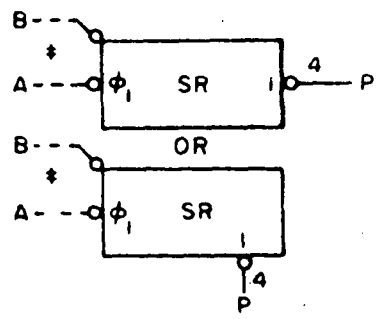
PATTERN NO. 6180 (ϕ_1 ϕ_2)

APRIL 1968

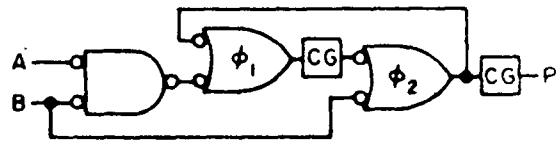
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_2 + \phi_2 \cdot \bar{B} \left[A_{t-1} B_{t-1} + \overline{B_{t-1}} P_{t-1} \right]$$

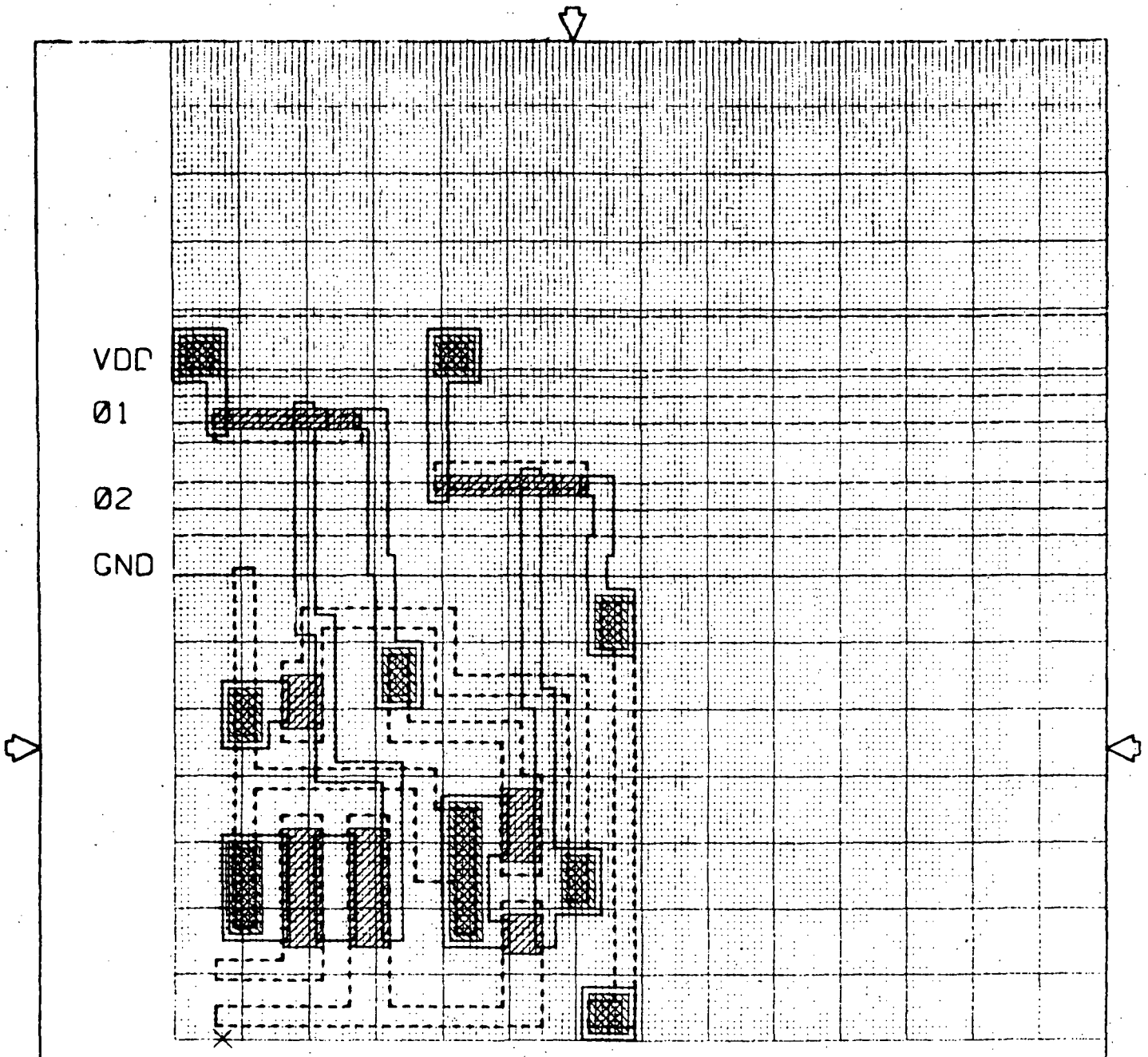
CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_P	4	440

PATTERN NO.

‡A IS AN INTERNAL INPUT CONNECTION FROM A 6140 OR 6160 CELL OUTPUT
B IS AN INTERNAL INPUT CONNECTION FROM B OF A 6140 OR 6160 CELL

STATIC REGISTER STRING END • 6180 • APRIL 1968



6180

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	STATIC REGISTER STRING END
SCALE 0.1mil/div		SHEET

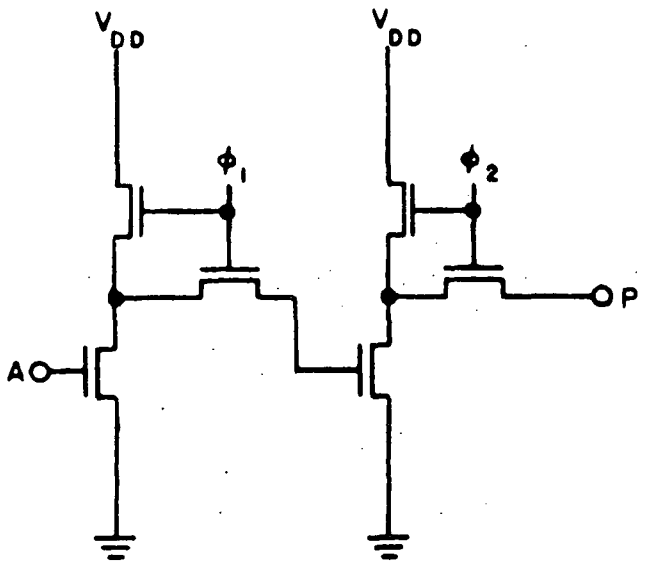
BANNING THICK OXIDE STANDARD CELL

DYNAMIC REGISTER STRING START

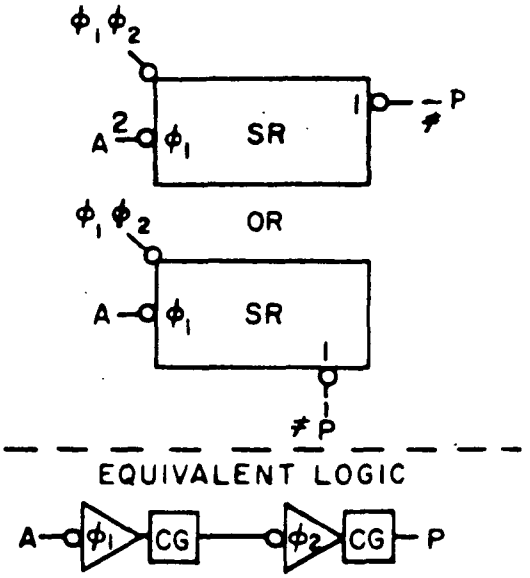
PATTERN NO. 6200 (ϕ_1 ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_1	ϕ_2	P
*	0	1	A_{t-1}
*	1	0	P_{t-1}

*MEANS EITHER STATE

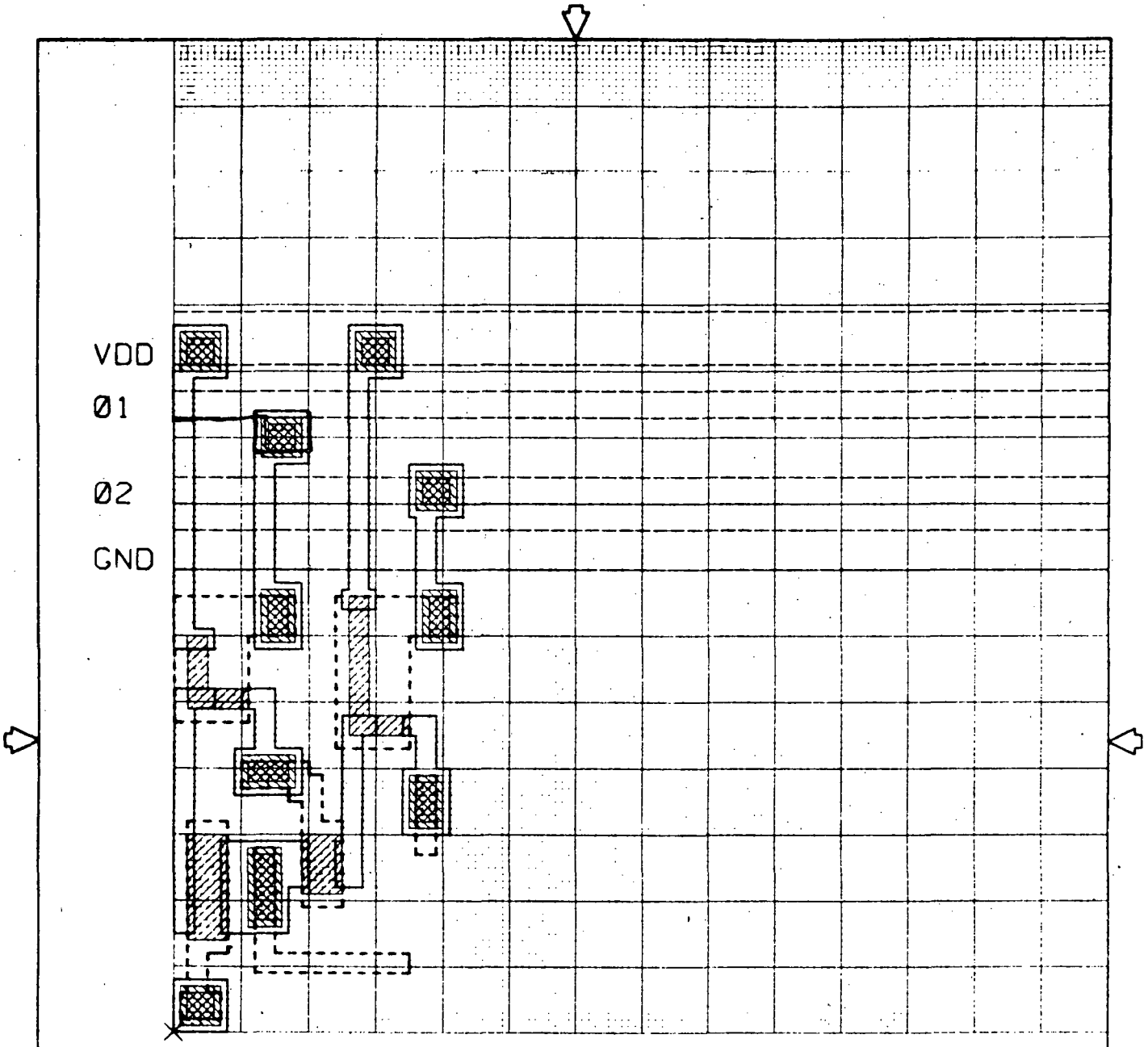
LOGIC EQUATIONS

$$P = (A_{t-1}) \cdot \phi_2 + (P_{t-1}) \cdot \phi_1$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	240
PATTERN NO.		6200

≠ P IS AN INTERNAL OUTPUT CONNECTION TO A 6220 OR 6240 CELL INPUT.



6200

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	**DYNAMIC REGISTER START**
SCALE **0.1mil/div**		SHEET

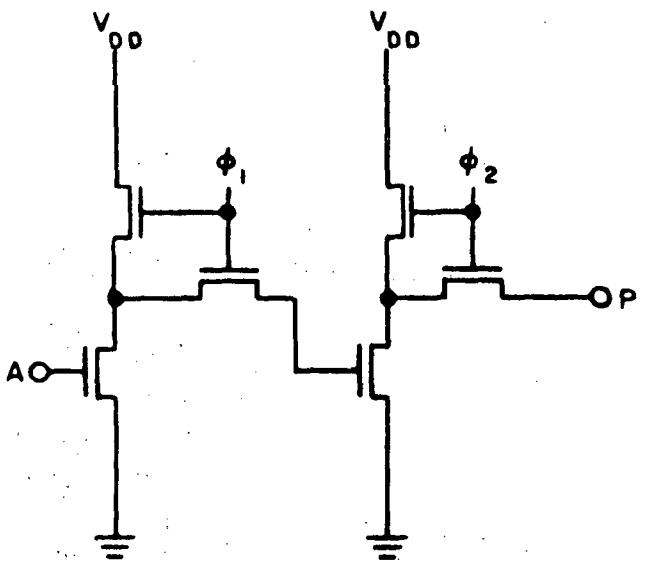
BANNING THICK OXIDE STANDARD CELL

DYNAMIC REGISTER STRING MIDDLE

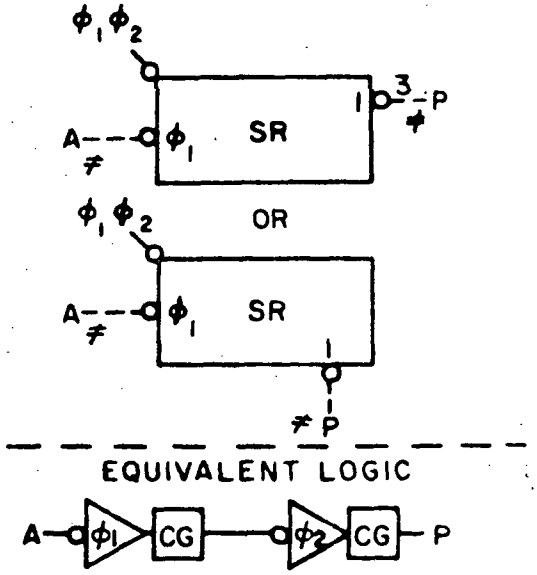
PATTERN NO. 6220 (ϕ_1 ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_1	ϕ_2	P
*	0	1	A_{t-1}
*	1	0	P_{t-1}

*MEANS EITHER STATE

LOGIC EQUATIONS

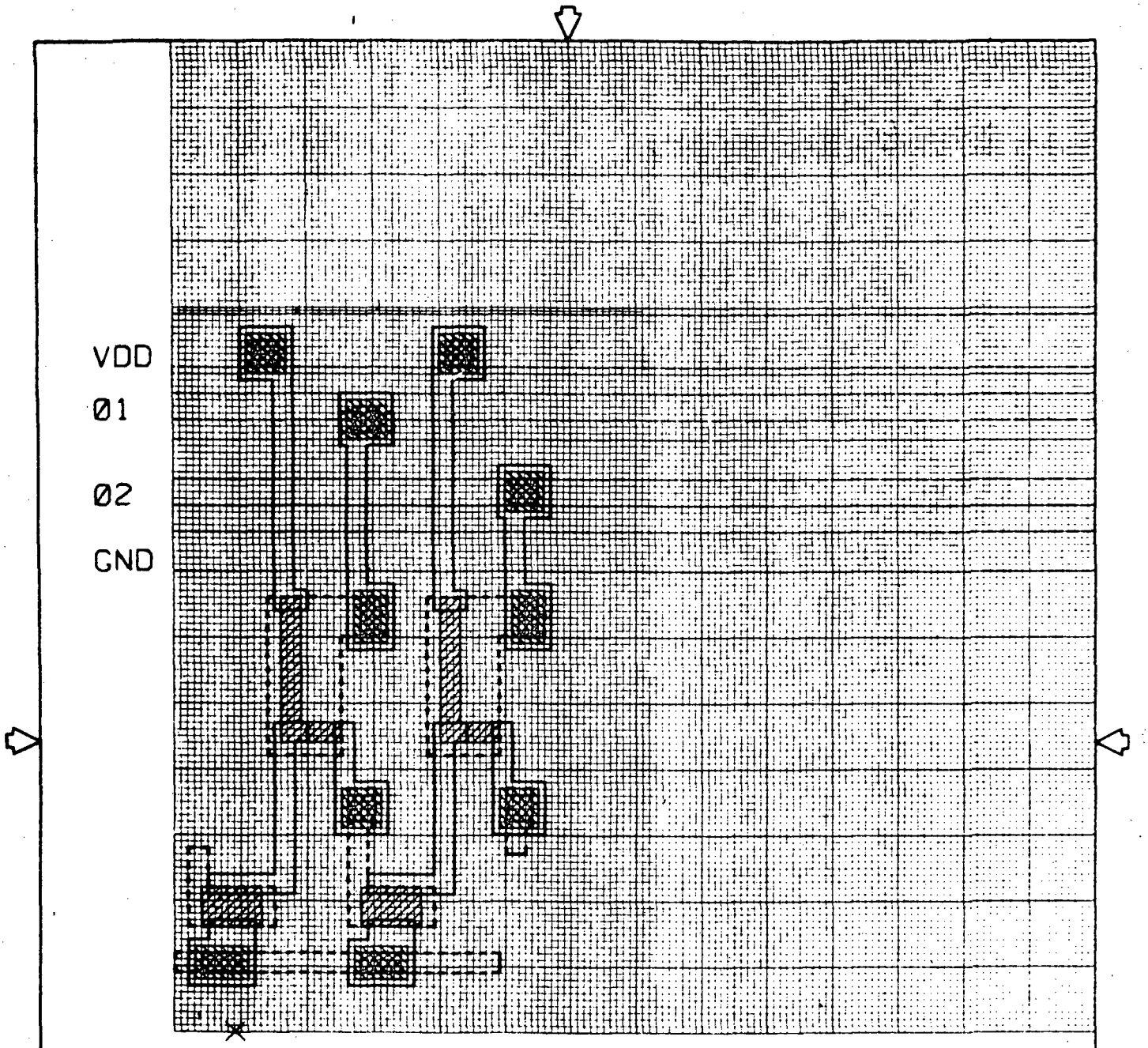
$$P = (A_{t-1}) \cdot \phi_2 + (P_{t-1}) \cdot \phi_1$$

CELL I/O CAPACITIES (NONE)

CAPACITOR	PIN	CAPACITY IN fF

PATTERN NO.

≠ A IS AN INTERNAL INPUT CONNECTION FROM A 6200 OR 6220 CELL OUTPUT.
P IS AN INTERNAL OUTPUT CONNECTION TO A 6220 OR 6240 CELL INPUT.



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	DYNAMIC REGISTER MIDDLE	
SCALE 0.1mil/div			SHEET

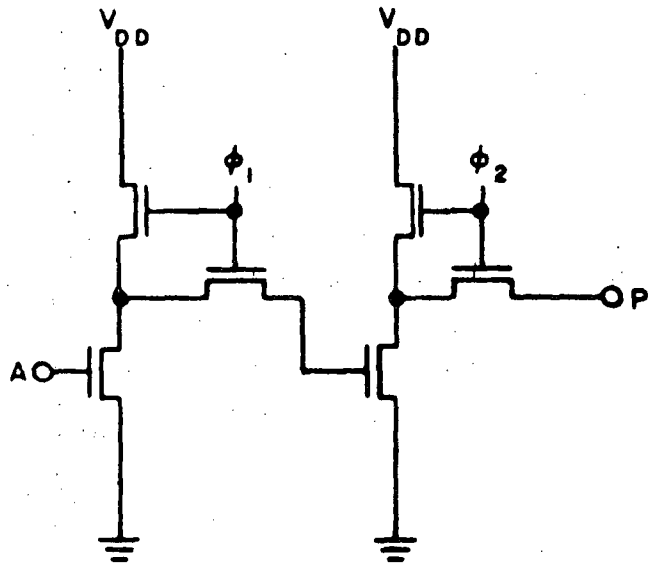
BANNING THICK OXIDE STANDARD CELL

DYNAMIC REGISTER STRING END

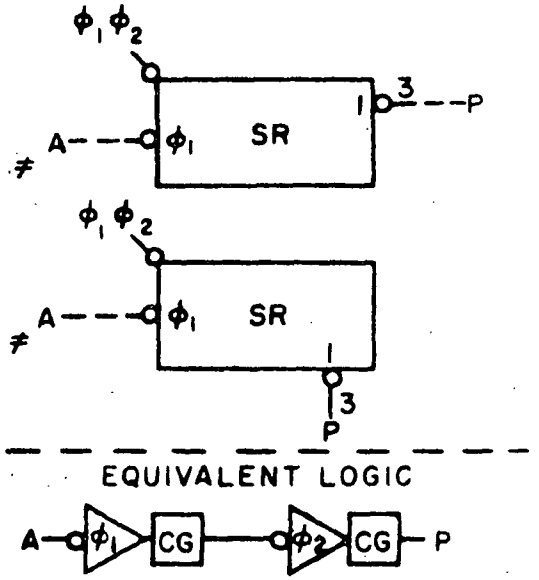
PATTERN NO. 6240 (ϕ_1 ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_1	ϕ_2	P
*	0	1	A_{t-1}
*	1	0	P_{t-1}

*MEANS EITHER STATE

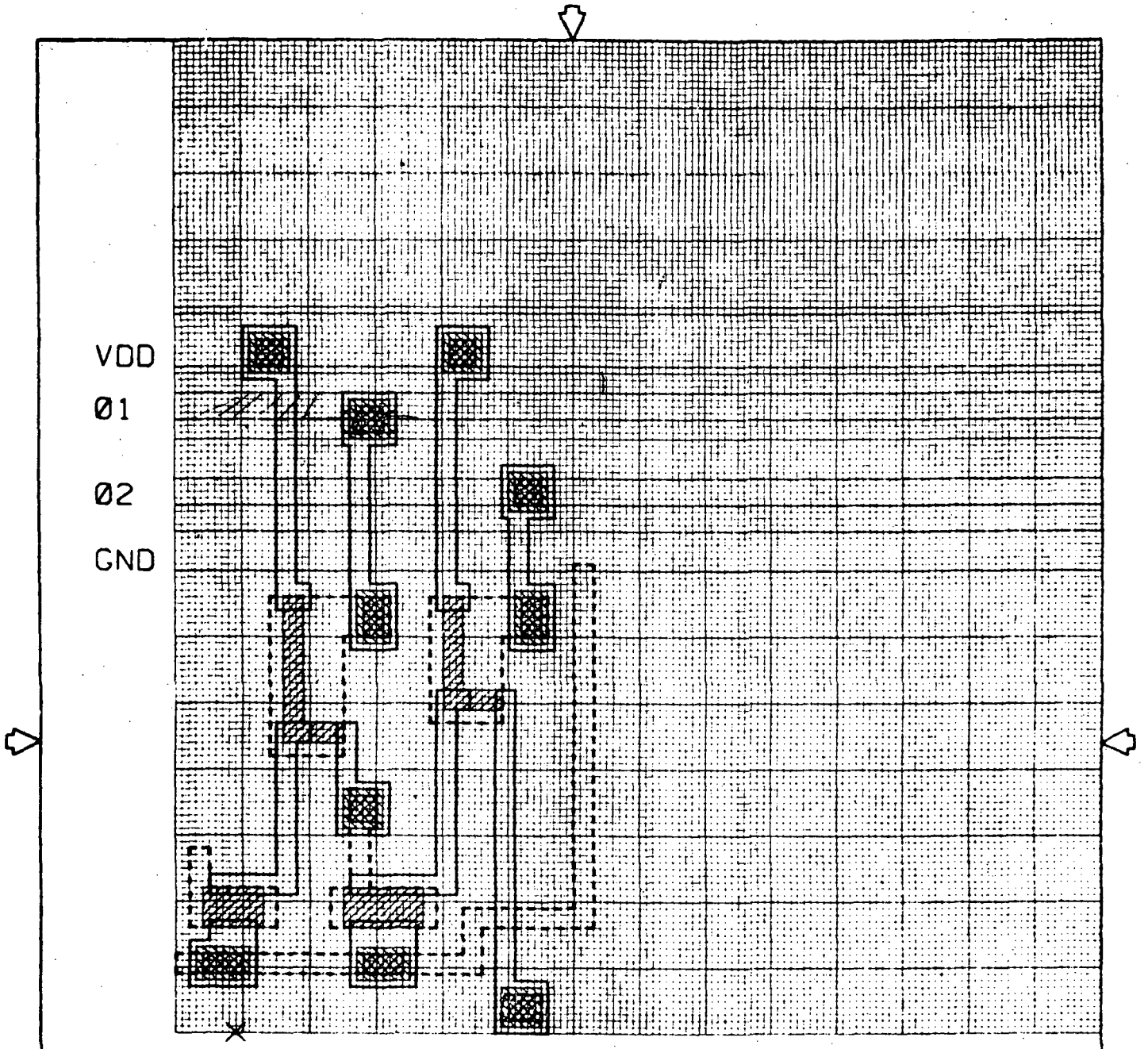
LOGIC EQUATIONS

$$P = (A_{t-1}) \cdot \phi_2 + (P_{t-1}) \cdot \phi_1$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_P	3	210
PATTERN NO.		6240

* A IS AN INTERNAL INPUT CONNECTION FROM A 6200 OR 6220 CELL OUTPUT.



6240

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	DYNAMIC REGISTER END
SCALE 0.1mil/div		SHEET

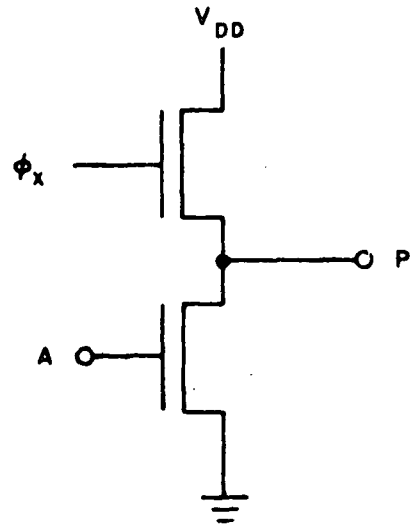
BANNING THICK OXIDE STANDARD CELL

INVERTER, 10pF

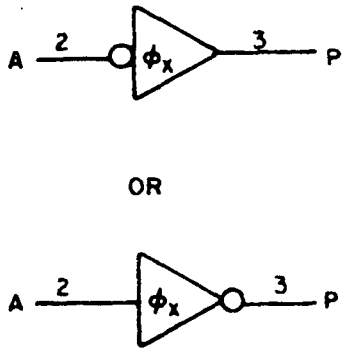
PATTERN NO. 6250 [ϕ_1]
6260 [ϕ_2]

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_x	P
0	0	P_{t-1}
1	*	0
0	1	1

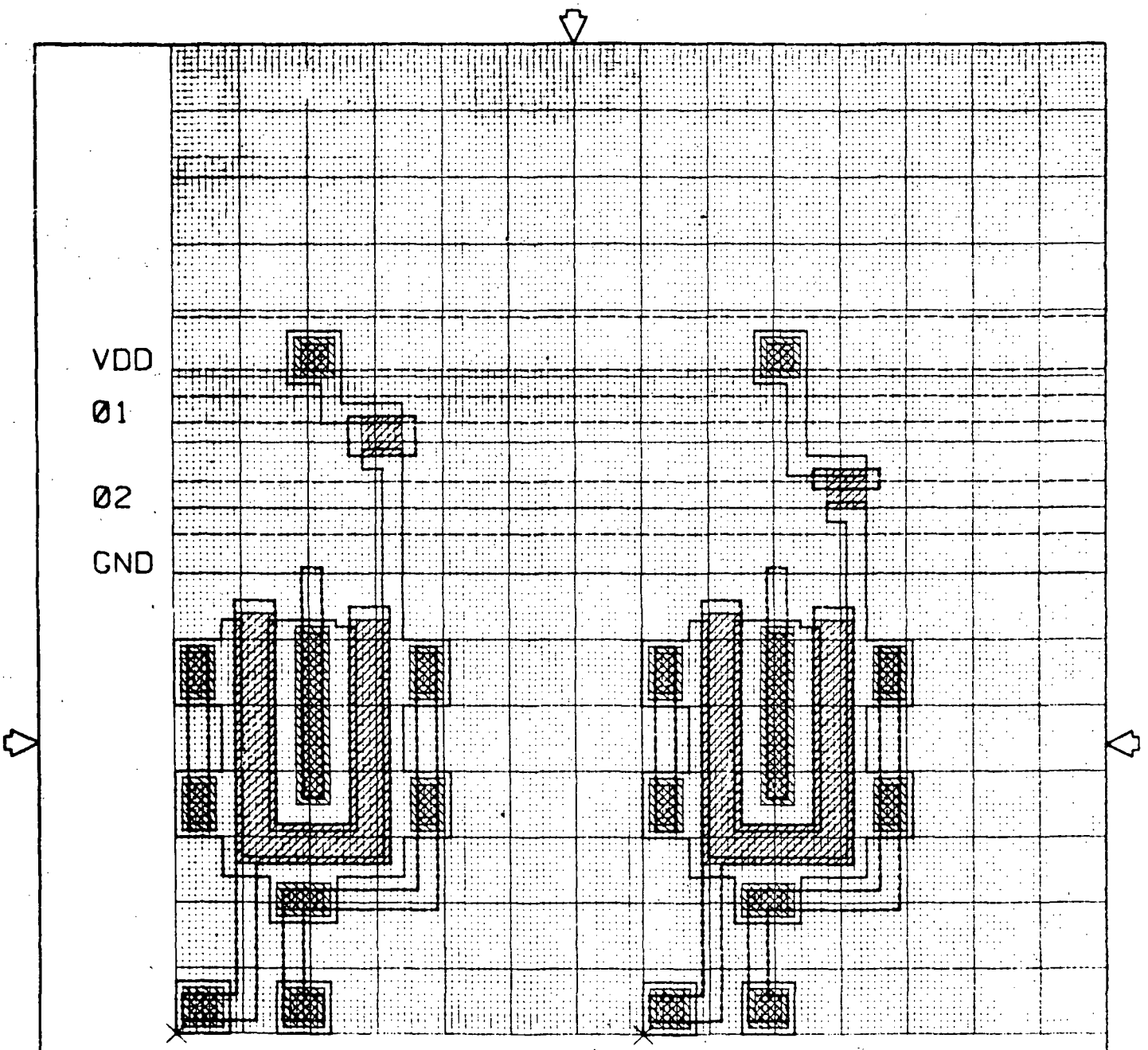
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot \bar{A} \cdot \bar{\phi}_x + \bar{A} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	2	1100	1100
C_P	3	600	560
PATTERN NO.		6250	6260



SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	10 Pf INVERTER	
SCALE 0.1mil/div			SHEET

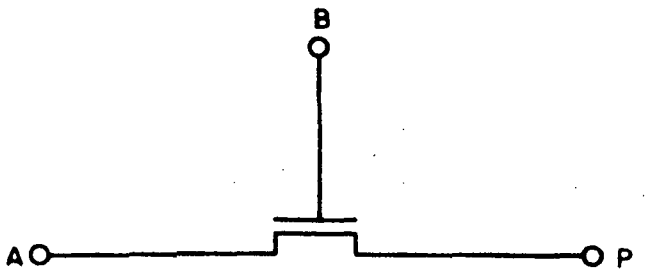
BANNING THICK OXIDE STANDARD CELL

ϕ_n CLOCK GATE

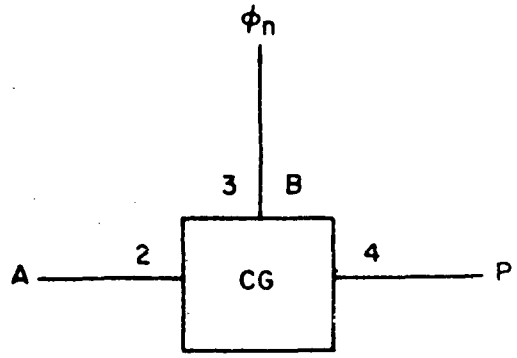
PATTERN NO. 6270

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_n	P
*	0	P_{t-1}
0	1	0
1	1	0

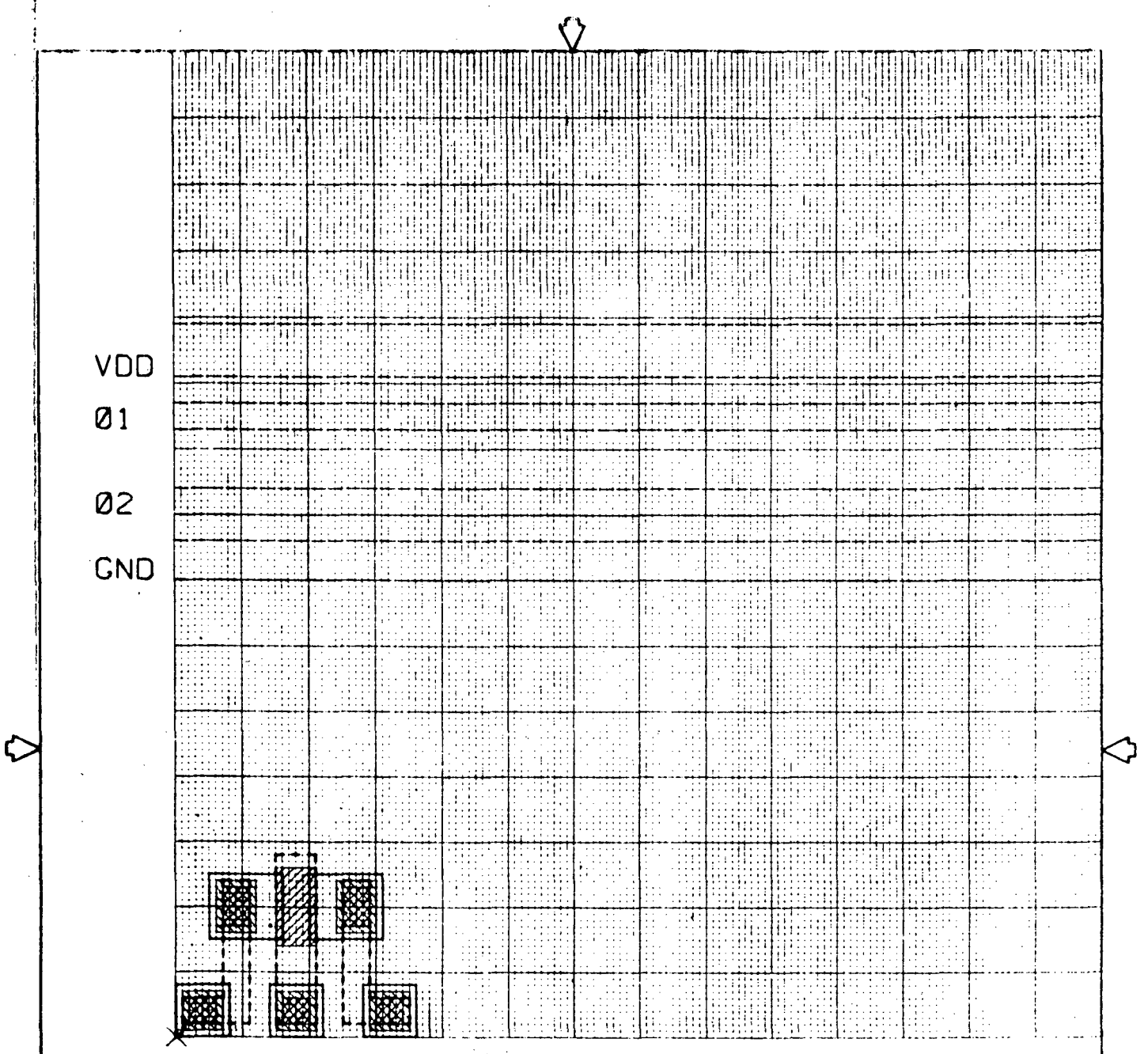
*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_n + A \cdot \phi_n$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	130
C_B	3	200
C_P	4	130
PATTERN NO.		6270



6270

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		**Ø n CLOCK GATE**
SCALE **0.1mil/div**			SHEET

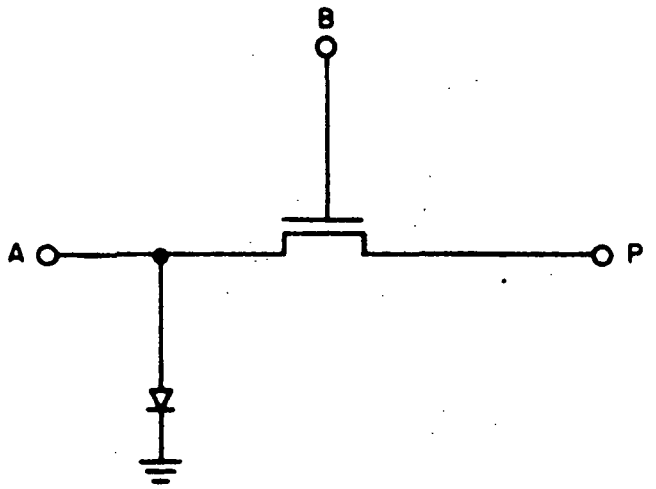
BANNING THICK OXIDE STANDARD CELL

ϕ_n PROTECTED CLOCK GATE

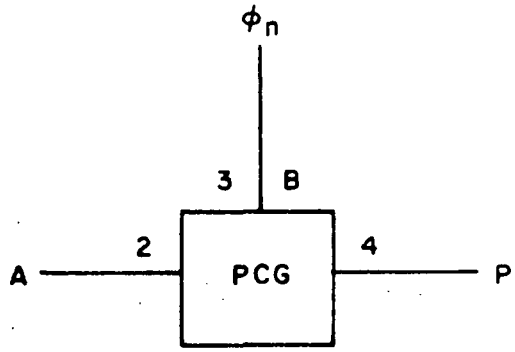
PATTERN NO. 6280

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_n	P
*	0	P_{t-1}
0	1	0
1	1	1

*MEANS EITHER STATE

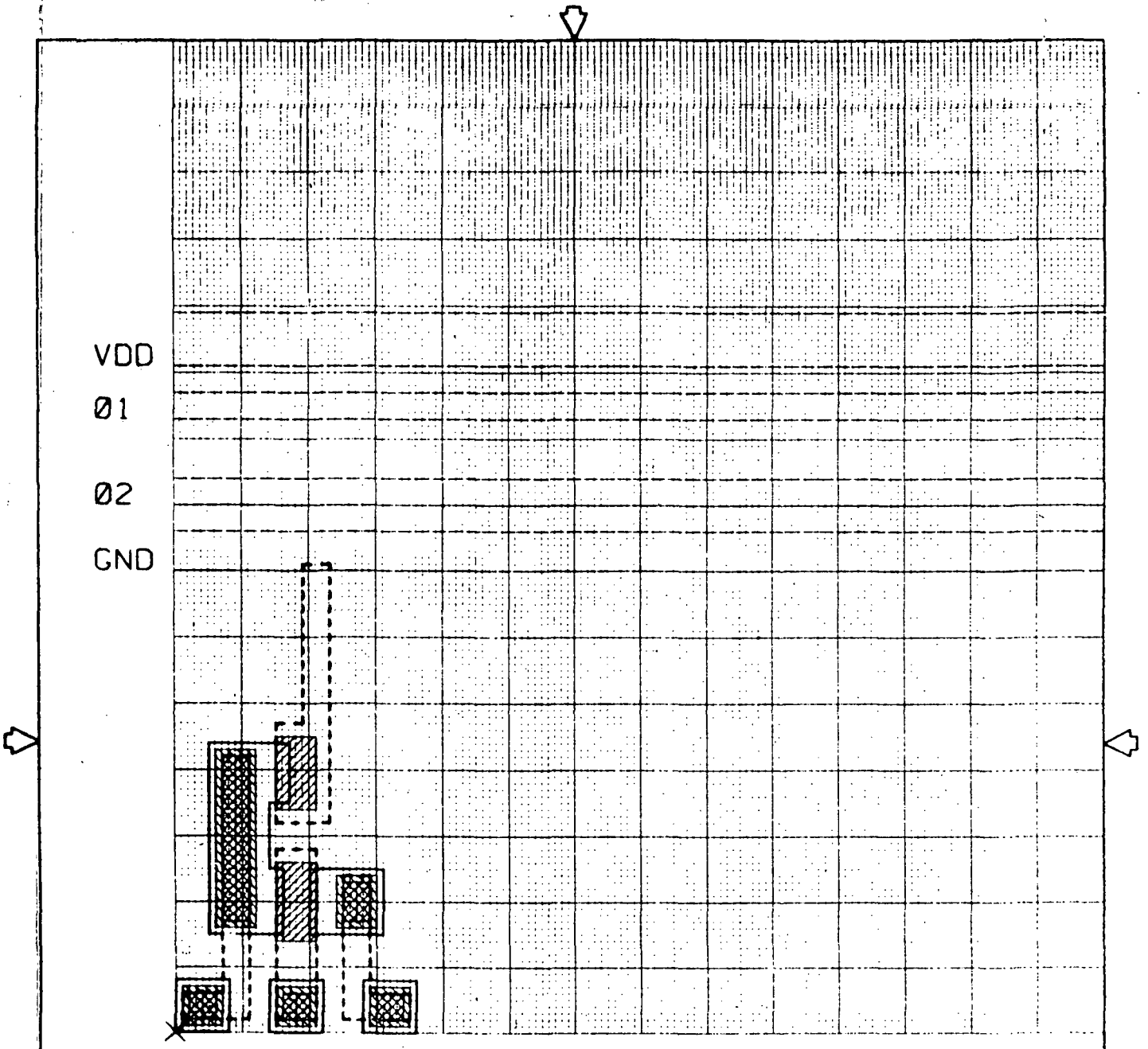
LOGIC EQUATIONS

$$P = P_{t-1} \cdot \bar{\phi}_n + A \cdot \phi_n$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	270
C_B	3	200
C_P	4	130
PATTERN NO.		6280

PROTECTED ϕ_n CLOCK GATE • 6280 • APRIL 1968



6280

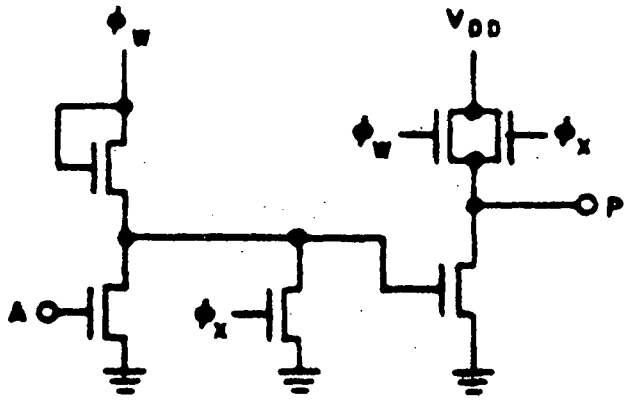
SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230		ØN PROTECTED CLOCK GATE
SCALE 0.1mil/div			SHEET

BANNING THICK OXIDE STANDARD CELL

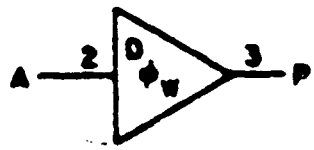
PRECHARGE BUFFER, 30pF — **PATTERN NO.** 6290 (ϕ_1) 6300 (ϕ_2)

JANUARY 1969

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	ϕ_w	ϕ_x	P
0	1	0	0
*	0	1	1
1	1	0	1

*MEANS EITHER STATE

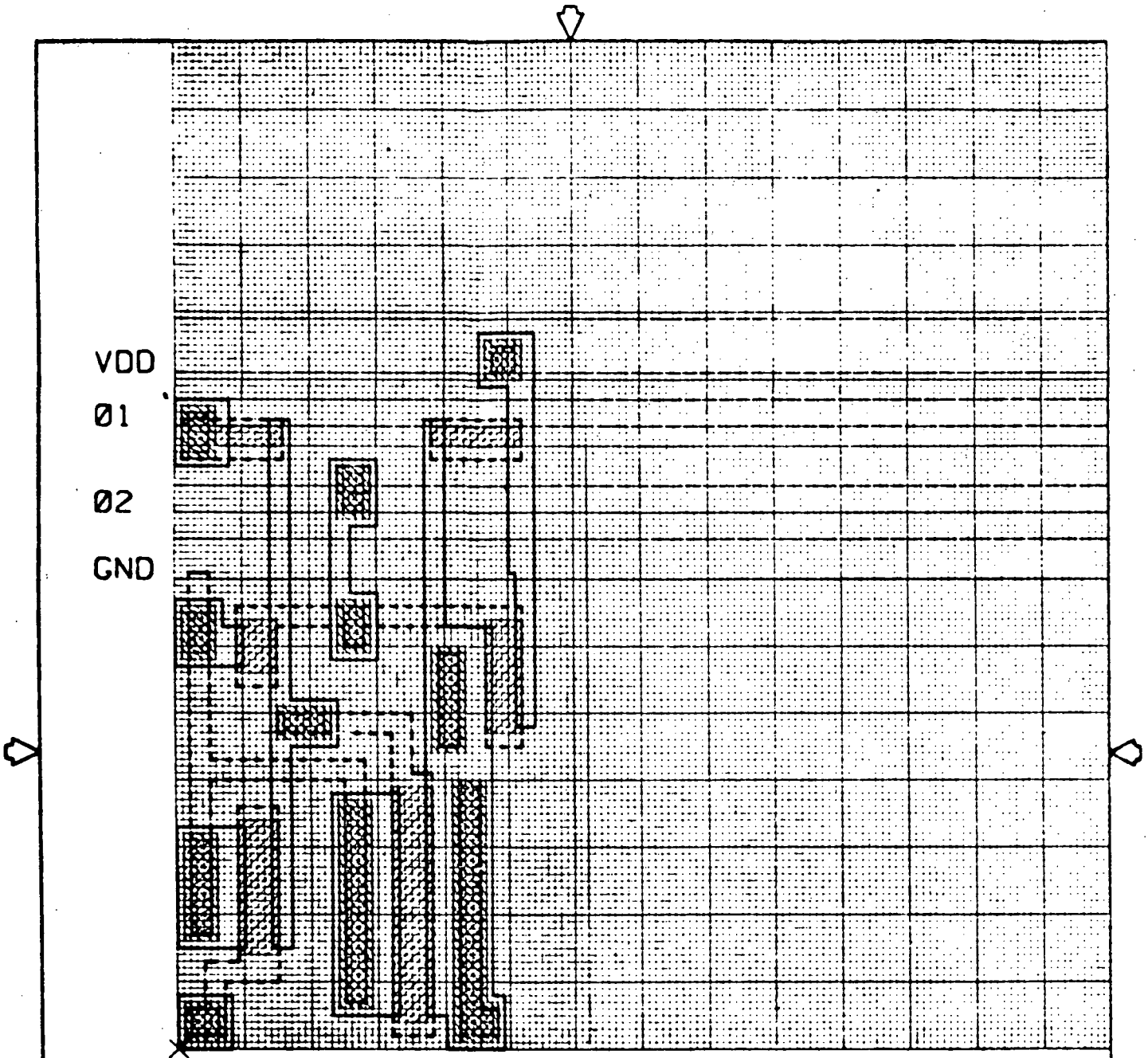
LOGIC EQUATIONS

$$P = A \cdot \phi_w + \phi_x$$

CELL I/O CAPACITIES

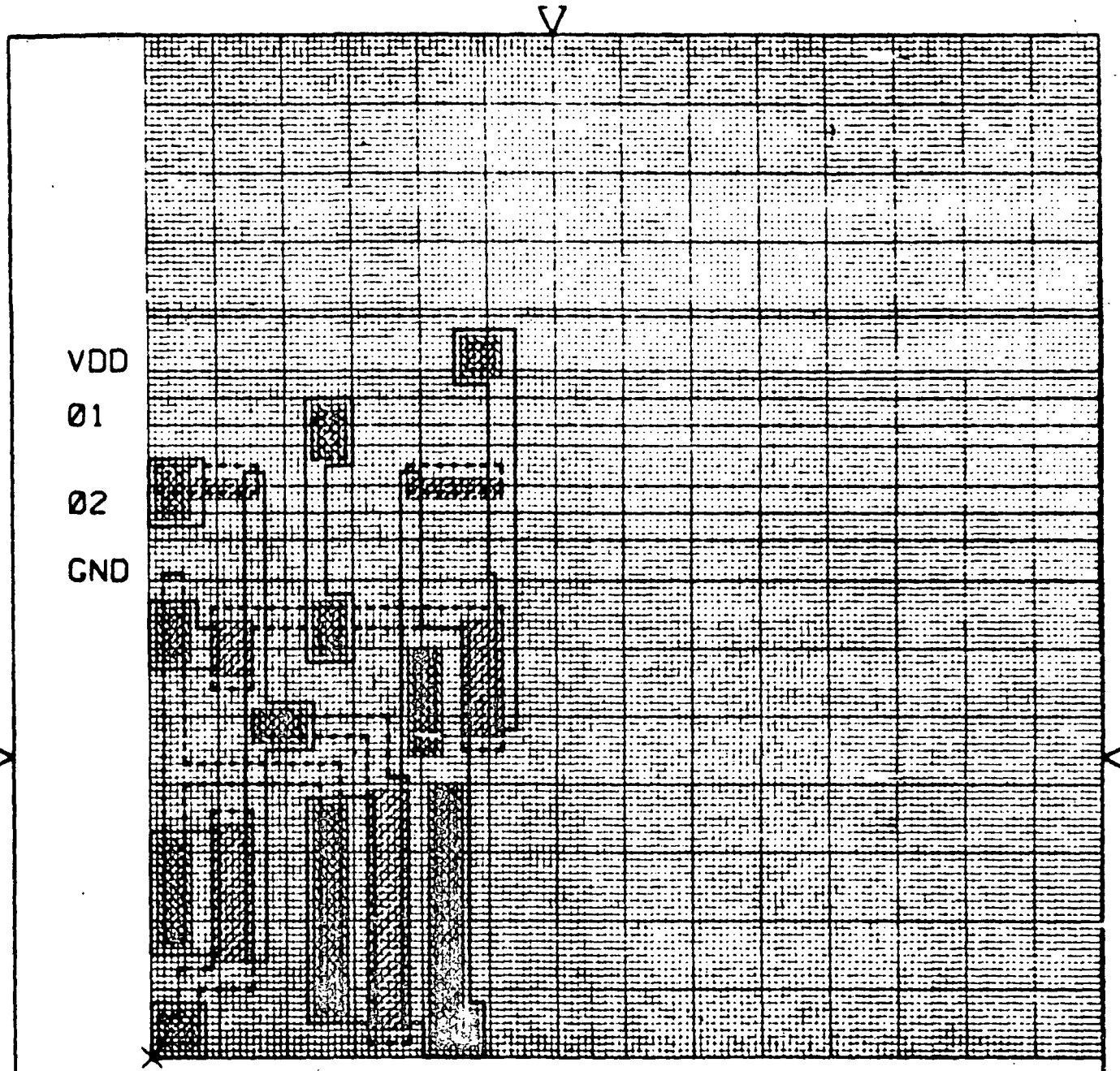
CAPACITOR	PIN	CAPACITY IN pF	
C_A	2	300	300
C_P	3	500	500
PATTERN NO.		6290	6300

30PF PRECHARGE BUFFER • 6290/6300 • JANUARY 1969



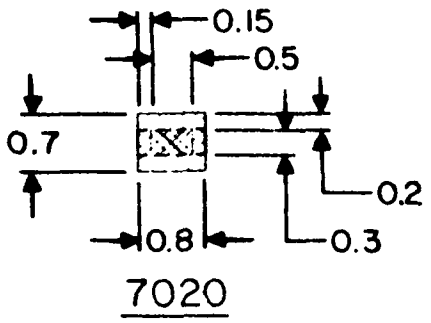
6290

SIZE	CODE IDENT. NO.	DWG. NO.	
A	98230	PRE- CHARGED BUFFER	(30 PF)
SCALE			SHEET

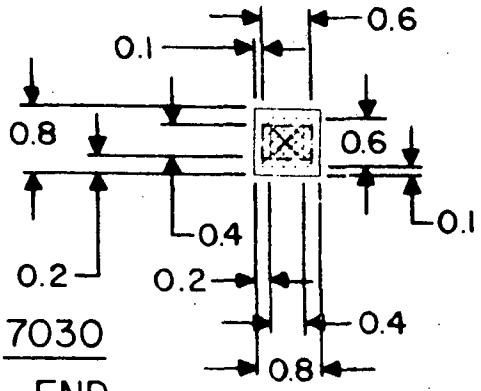


6300

SIZE	CODE IDENT.NO.	DWG.NO.	
A	98230	PRE-CHARGED BUFFER (30PF)	
SCALE			SHEET

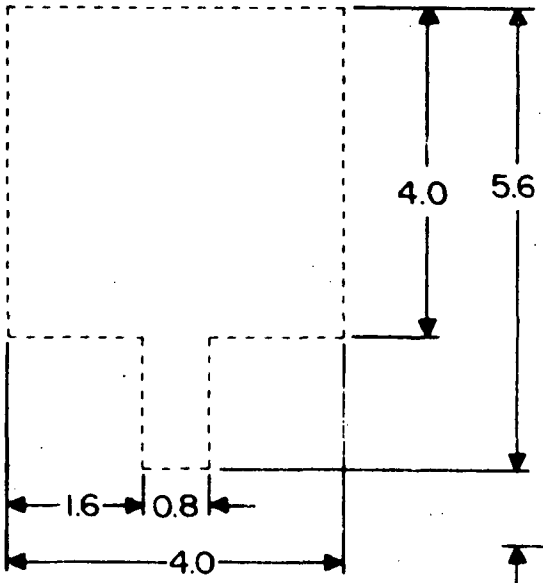


7020



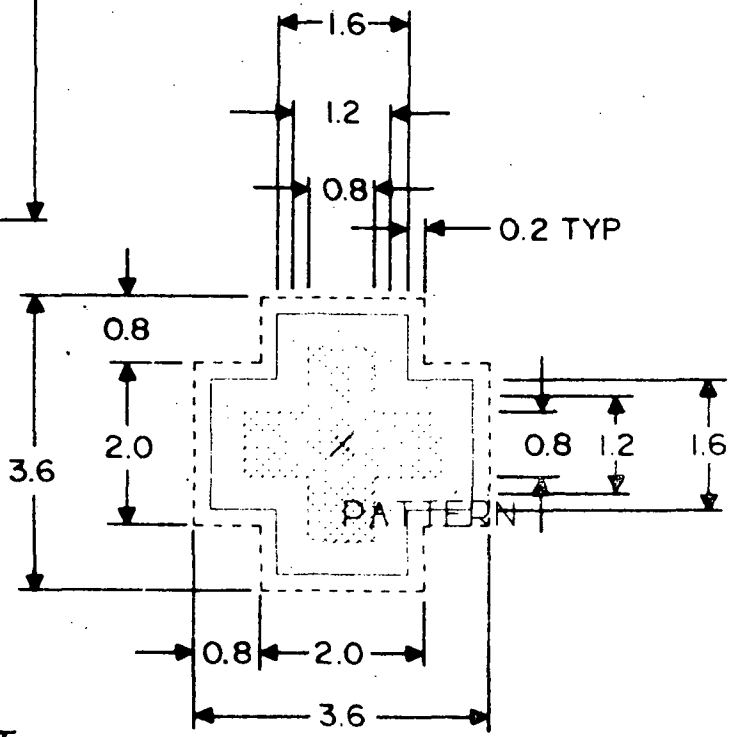
7030

TUNNEL END



9034

PAD



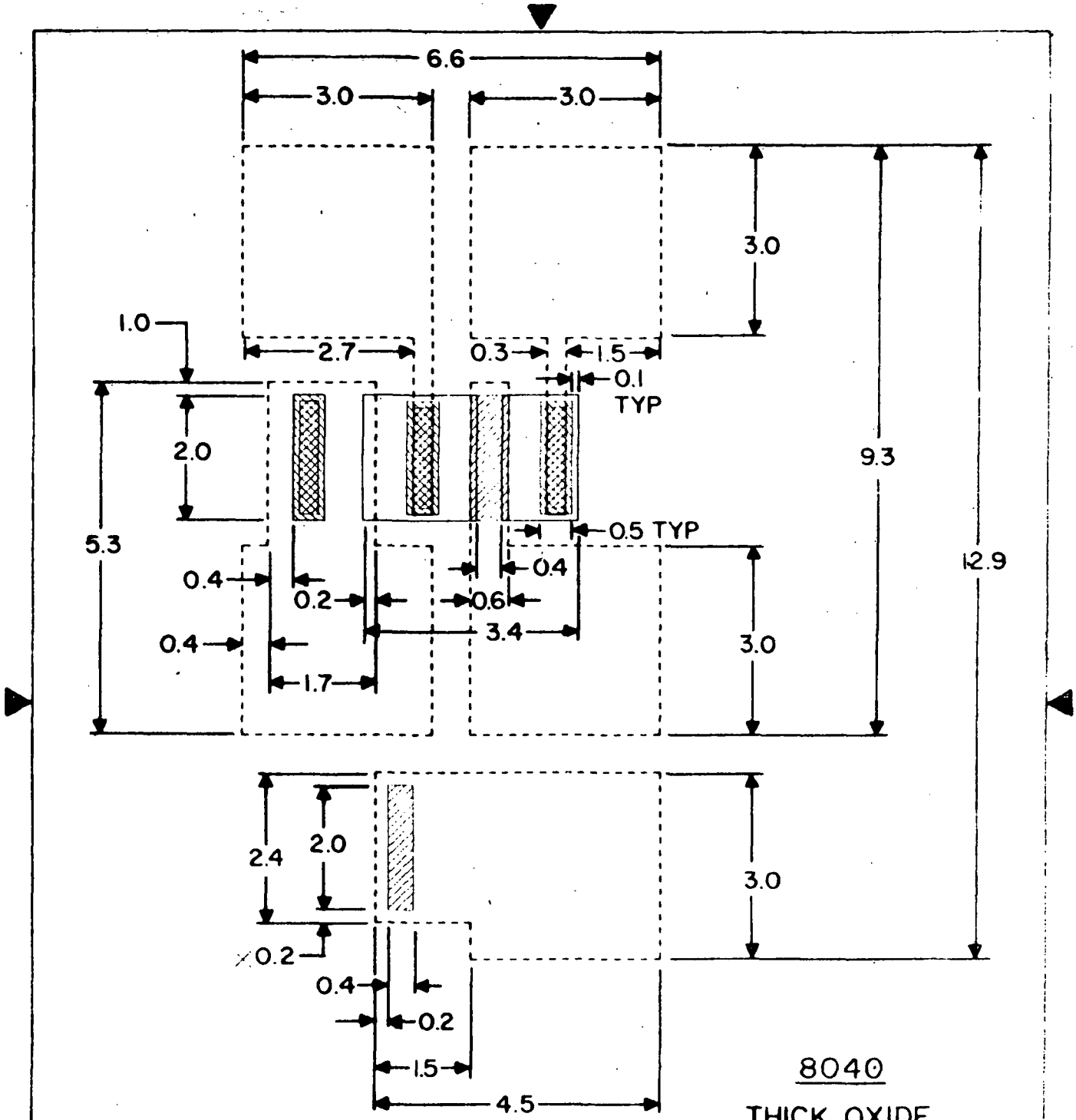
7510

ON CHIP

ALIGNMENT

PATTERN

SIZE	CODE IDENT. NO.	DWG. NO.
A	98230	MISC. PATTERNS
SCALE 2 MILS = 1 INCH		SHEET

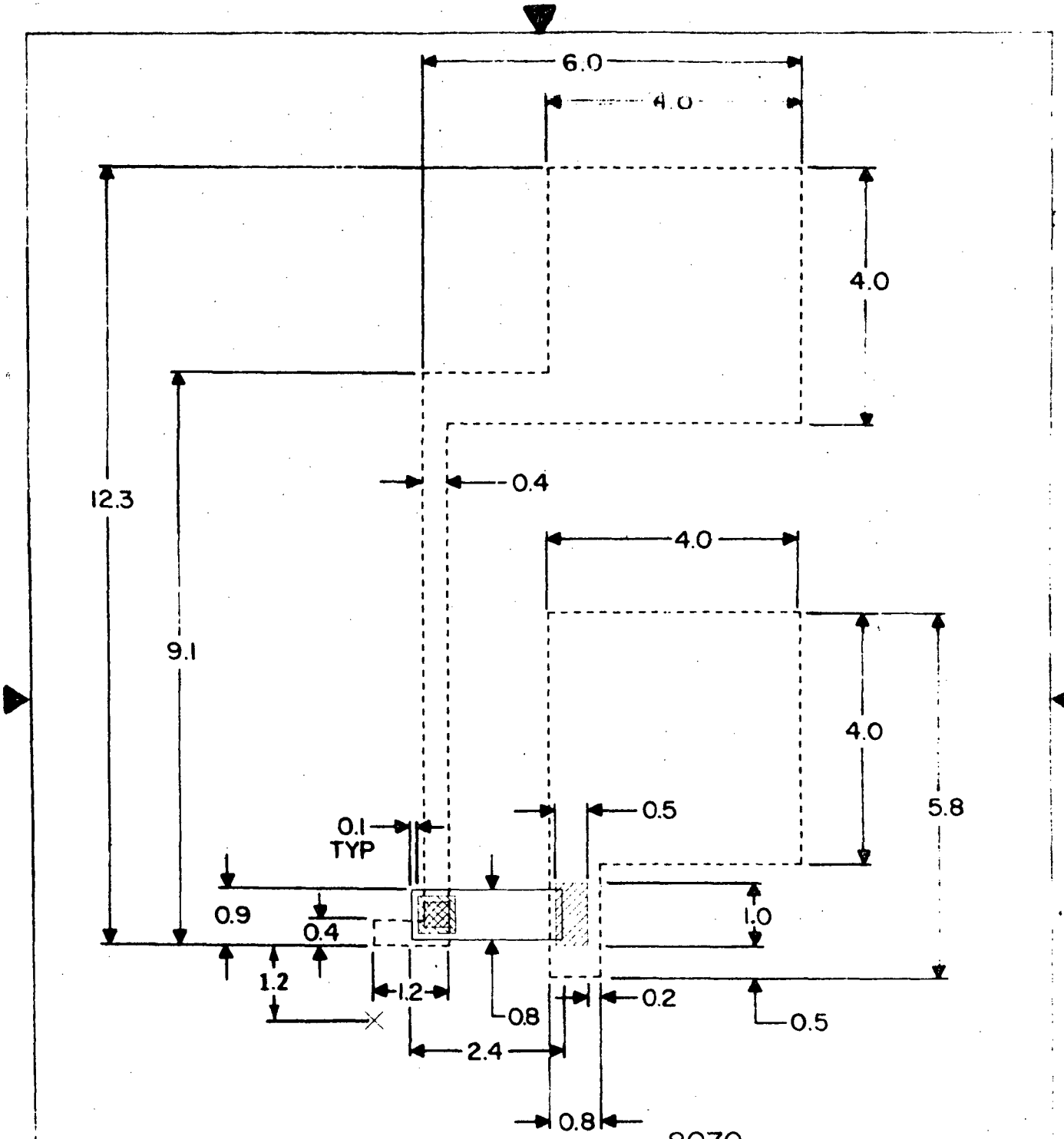


8040

THICK OXIDE

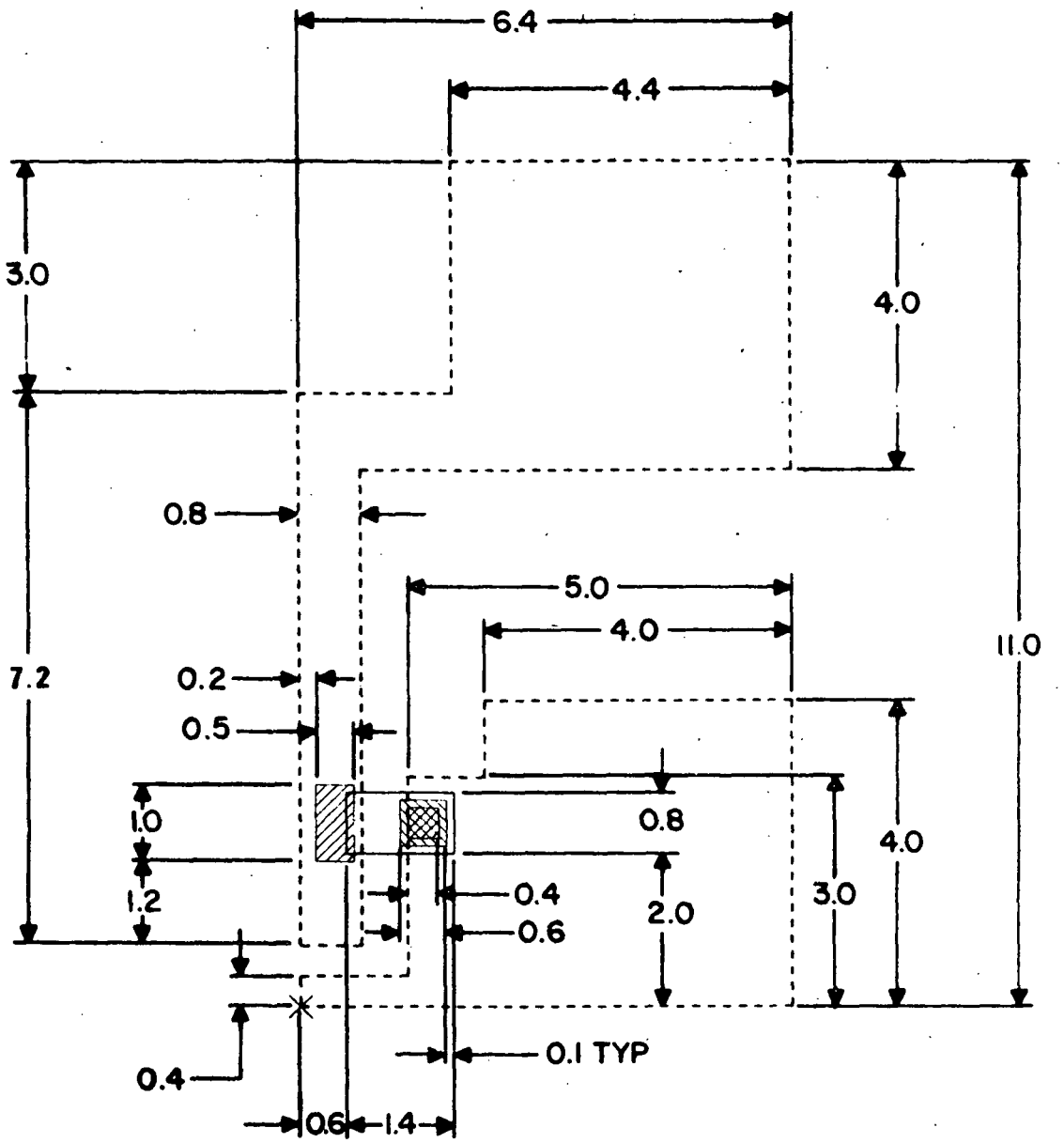
TEST TRANSISTOR

SIZE	CODE IDENT. NO	DWG. NO.
A	98230	MISC. PATTERNS
SCALE 2 MILS = 1 INCH		SHEET



8070
$\emptyset_1, V_{DD}$ PAD
PATTERN

SIZE	CODE IDENT. NO.	DWG. NO.
A	98230	MISC. PATTERNS
SCALE 2 MILS = 1 INCH		SHEET



8080

$\emptyset_2$, GND PAD PATTERN

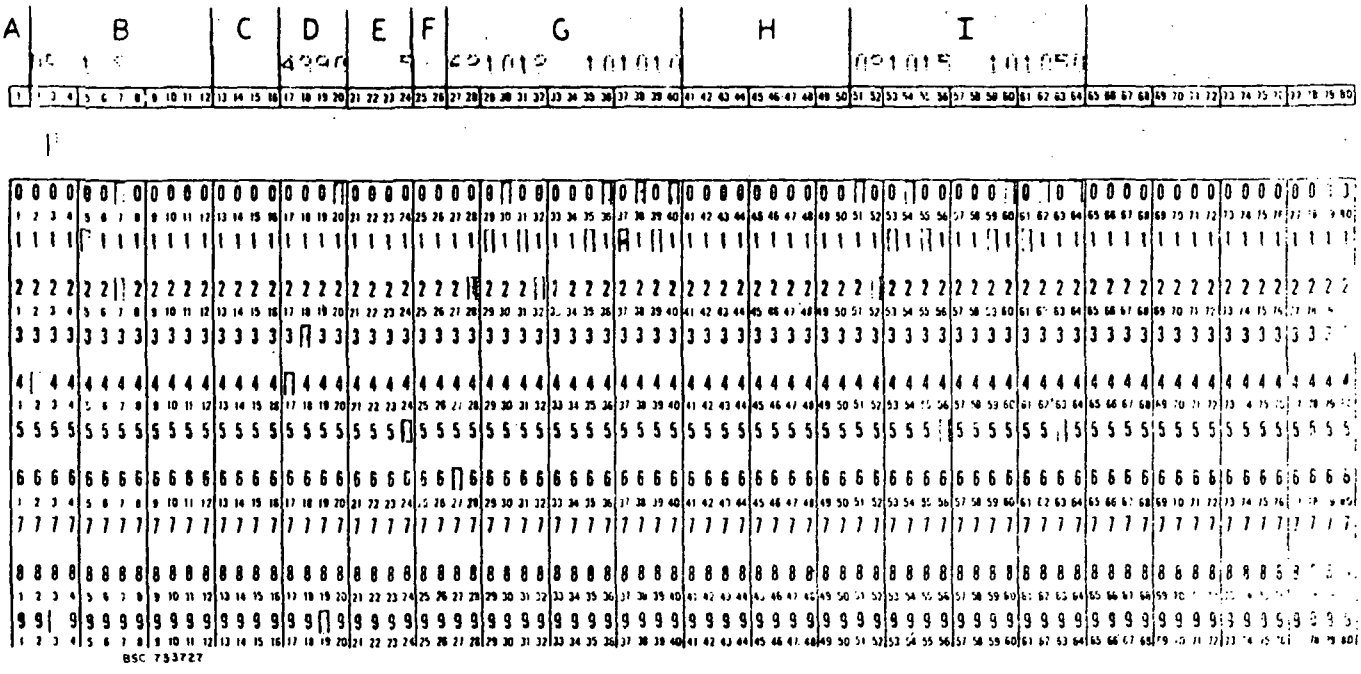
SIZE	CODE IDENT. NO.	DWG. NO.
A	98230	MISC. PATTERNS
SCALE 2 MILS = 1 INCH		SHEET

C. Circuit-Type File

Each cell or pattern type which has been designed and placed on the PATTERN LIBRARY tape requires a definition for use by the PLACEMENT-ROUTING-FOLDING program, the LOGBLOSIM V program, the SPEED ANALYSIS subroutine and the LOGBLOSIM V to PLACEMENT-ROUTING-FOLDING CONVERT routine. Each cell pattern definition requires n+1 cards, where n is the number of pins in the cell.

The first card is the pattern card. This card supplies the name and pattern number of the cell and specifications required for the cell-spacing subroutine.

Figure 1 - Card as it Appears:



Coded Breakdown:

Field A, Column 1, Blank.

Field B, Columns 2 through 12.

Circuit name. The name may be any 11-character alphanumeric designation.

Field C, Columns 13 through 16.

Alphanumeric-mneumonic cell type identifier for future use by LOGBLOSIM V and CONVERT routine.

Field D, Columns 17 through 20.

Pattern number. Must be equivalent to the family pattern number in the Artwork Program library of standard patterns.

Field E, Columns 21 through 24.

Number of pins in the pattern; two plus the number of input- plus output-tunnel ends.

Field F, Columns 25 and 26. Blank.

Field G, Columns 27 through 40.

Right edge cell spacing.

Field H, Columns 41 through 50. Blank.

Field I, Columns 51 through 64.

Left edge cell spacing.

The data for the SPACE Subroutine in fields G and I describe the edges of the cell. Each vertical side of the cell is divided into 6 regions as shown in figure 2:

1. Input or output tunnel end - between 0.0 and .8 mil from the bottom of the cell.
2. Lower metal region - between .8 mil and 4.3 mils from the bottom of the cell.

3. Lower p region - between .8 mil and 4.5 mils from the bottom of the cell.
4. Upper metal region - between 3.5 mils from the bottom of the cell and the ground buss.
5. Upper p region - between 3.3 mils from the bottom of the cell and the ground buss.
6. Buss region - above the bottom of the ground buss.

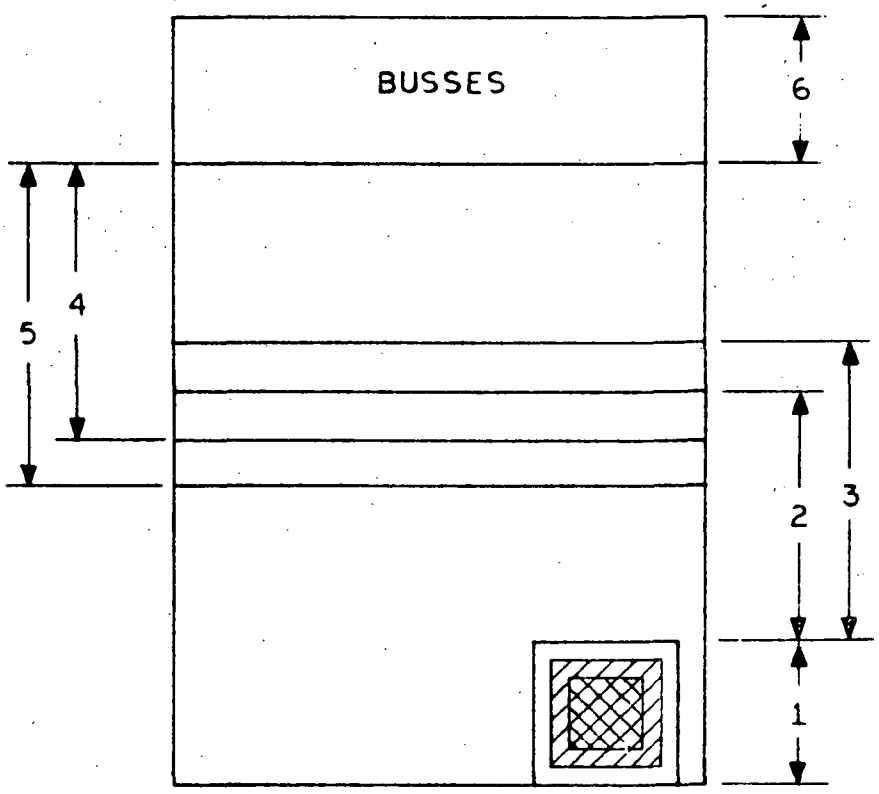


FIGURE 2

The data required is in two categories:

1. The distance from the edge of the cell to the metal or p region closest to the edge.
2. The potential of the material described above.

The data must be in accord with the following ground rules:

1. All distances are in tenths of mils.
2. If a distance is greater than .9 mils, assume it is .9 mils.
3. For potential, enter 0 for ground and 1 for non-ground.
4. If a region has material at ground near the edge of the cell and another piece of material not at ground farther but less than .6 mil from the edge, enter the distance to the region closest to the edge and a potential of 1.
5. Gate oxide regions are assumed to be p regions since the same design rules apply.
6. For p or gate oxide regions extending into the V_{DD} buss, enter 5 unless the material is a type 6 tunnel end as shown in figure 3. In this case enter 6.

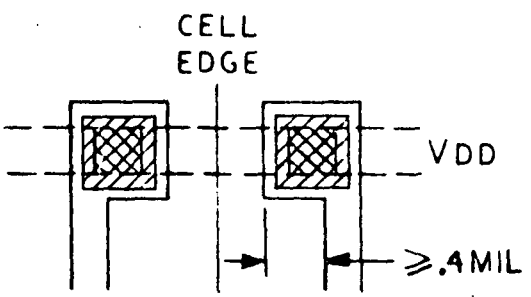


Figure 3 - Type 6 tunnel ends

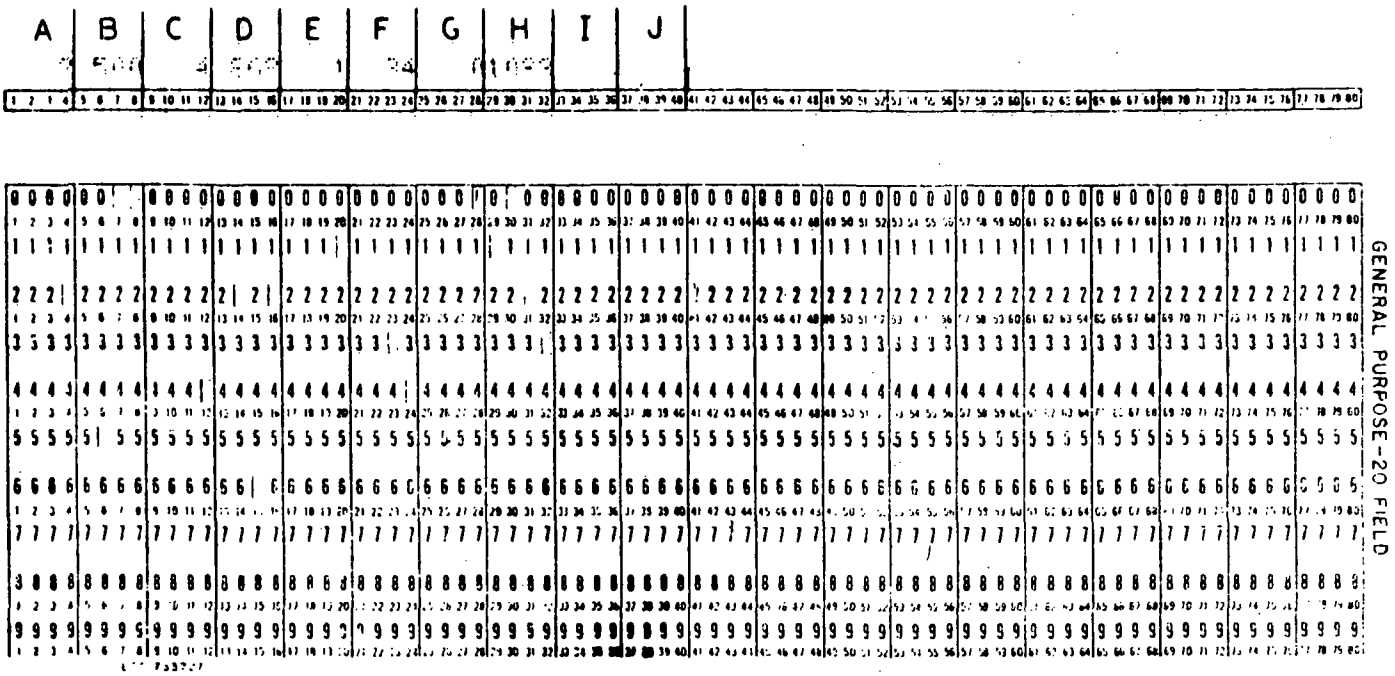
Table 1 shows the order in which the data is entered:

TABLE I

COLUMN NUMBER RIGHT EDGE	COLUMN NUMBER LEFT EDGE	ABBREVIATION	DESCRIPTION
27	51	DP	Distance from cell edge to tunnel end.
28	52	DLM	Distance from cell edge to the metal closest to the edge in the lower metal region.
29	53	PLM	Potential of lower metal.
30	54	DLP	Distance from cell edge to the p region closest to the edge in the lower p region.
31	55	PLP	Potential of lower p region.
32	56	DUM	Distance from cell edge to the metal closest to the edge in the upper metal region.
35	59	PUM	Potential of upper metal.
36	60	DUP	Distance from cell edge to the p region closest to the edge in the upper p region.
37	61	PUP	Potential of upper p region.
38	62	DB	Distance from cell edge to the p region in the buss area closest to the edge.
39	63	TB	Buss nearest the top of the cell which covers the material described above. Enter 1 for ϕ_1, 2 for ϕ_2, and 5 for V_{DD} except as noted in ground rule 6.
40	64	DMB	Distance from edge of cell to any metal which is connected to the ϕ_1 or ϕ_2 busses but extend either down or up from the .4 mil buss line.

The remaining cards are pin cards used to define cell-pin parameters.

Figure 4 - Card as it Appears:



Coded Breakdown:

Use one card for each pin.

Field A, Columns 1 through 4.

Pin number. Input/Output pins are numbered left to right on the layout (pins 2 to n-1). The left edge of the cell is pin 1, and the right edge of the cell is pin n.

Field B, Columns 5 through 8.

Reassignment flag. The numbers in this field of the Circuit Type File provide information for the ROUTE and SIGNAL TRACE subroutines of the PLACE-ROUTE and FOLD program. If two are the same the WIRE ROUTE program may interchange them when the

orientation of the cell is selected. For the SIGNAL TRACE routine the number describes the node to which the pin is connected. It is constructed by summing the following values:

1. 0, 2, ..., 14 for a phase two node with no internal killer or
   1, 3, ..., 15 for a phase one node with no internal killer or
   16, 18, 20, 22 for a phase two node with an internal killer or
   15, 17, 19, 21 for a phase one node with an internal killer or
   23 for a phase one static or dynamic register cell or
   24 for a phase two static or dynamic register cell.
2. 50 for an output pin.
3. 100 for an internal clock gate at the node.
4. $100.2^N + 100.2^M$ for inputs connected to the Nth and Mth nodes, counting from the last or
   $100.2^N + 100.2^M$ for outputs connected to the Nth node and feeding back to the Mth node, counting from the start.

   Ex. number 750 indicates: (1) phase 2, no killer
   (2) output pin
   (3) internal clock gate
   (4) connection to the second node and feed back to the first.

   The five special cells (ϕ_1, ϕ_2, ϕ_N killer, ϕ_N clock gate and Pad) numbers are assigned according to the special function of the individual pin.

Field C, Columns 9 through 12.

Distance from the center of the pin to the center of the pin to the left, in tenths of mils.

Field D, Columns 13 through 16.

Capacitance of pin, in picofarads times 1000, e.g., 1.4 pF is punched as 1400.

Field E, Columns 17 through 20.

Each number shows which input or output in the LOGBLOSIM V program corresponds to the pin. The inputs are numbered the same as the input field number in the LOGBLOSIM V program. The outputs are numbered 1 for primary, 2 for secondary and 3 for tertiary.

Field F, Columns 21 through 24.

Constant times 10 used for SPEED ANALYSIS program. $K = C_L/t$. t is the pair delay of the cell and C_L is the load on the output. Maximum pair delay is .3 microseconds. The maximum capacity the cell can drive is then .3K, e.g., if field F = 143 the cell is capable of driving (14.3) (.3) = 4.29 pf.

Field G, Columns 25 through 28.

Correction factor times 100 used by SPEED ANALYSIS program when the output of the cell is driving through a clock gate. If C_{L1} is the load capacity before the clock gate and C_{L2} is the load capacity after the clock gate the effective load is $C_{Leff} = C_{L1} + (C.F.)\ (C_{L2})$.

Field H, Columns 29 through 32.

This is a means of entering internal node capacity for the SPEED ANALYSIS program. It is entered in picofarads times

1000 on all the input pins of the circuit driving the internal node.

Field I, Columns 33 through 36.

Gate to drain capacitance in picofarads times 1000 of all inputs (upper input only on NAND structure) used by SIGNAL TRACE program in determination of acceptable capacitance feedback ratios.

Field J, Columns 37 through 40.

Minimum capacitance to ground in picofarads times 1000 of all inputs and outputs. This is calculated using gate masks which do not overlap source or drain P-material (MASK 5) on the input pins and assuming all coupling devices are not conducting on the outputs. This is used by the SIGNAL TRACE program in determining acceptable capacitance feedback ratios for cell inputs.

The following sheets contain the circuit type file:

CIRCUIT TYPE FILE JUNE 1969

2 NOR		2070	5	61614	20666		0	61612		66		0
1	0	0	0	0	0	0	0	0	0			
2	201	4	290	1	0	0	0	58	203			
3	251	14	296	1	73	106	0	0	296			
4	201	14	291	2	0	0	0	58	203			
5	0	4	0	0	0	0	0	0	0			
2 NOR		2080	5	61614	20666		0	61612		66		0
1	0	0	0	0	0	0	0	0	0			
2	200	4	290	1	0	0	0	58	203			
3	252	14	271	1	73	106	0	0	271			
4	200	14	291	2	0	0	0	58	203			
5	0	4	0	0	0	0	0	0	0			
2 NOR DEL		2090	5	21612	111513		0	31013	101066			0
1	0	0	0	0	0	0	0	0	0			
2	301	4	358	1	0	0	0	85	249			
3	301	14	361	2	0	0	0	85	249			
4	351	14	483	1	71	111	0	0	159			
5	0	4	0	0	0	0	0	0	0			
2 NOR DEL		2100	5	21612	111523		0	31013	101066			0
1	0	0	0	0	0	0	0	0	0			
2	300	4	358	1	0	0	0	85	249			
3	300	14	361	2	0	0	0	85	249			
4	350	14	445	1	71	111	0	0	140			
5	0	4	0	0	0	0	0	0	0			
3 NOR		2110	6	41314	131666		0	61612		66		0
1	0	0	0	0	0	0	0	0	0			
2	201	4	291	1	0	0	0	58	203			
3	201	14	288	2	0	0	0	58	203			
4	201	14	288	3	0	0	0	58	203			
5	251	14	461	1	73	106	0	0	461			
6	0	4	0	0	0	0	0	0	0			
3 NOR		2120	6	41314	131666		0	61612		66		0
1	0	0	0	0	0	0	0	0	0			
2	200	4	291	1	0	0	0	58	203			
3	200	14	288	2	0	0	0	58	203			
4	200	14	288	3	0	0	0	58	203			
5	250	14	436	1	73	106	0	0	436			
6	0	4	0	0	0	0	0	0	0			

CIRCUIT TYPE FILE JUNE 1969

3 NOR DEL		2130	6	1500	101513		0	31013	101066		0
1	0	0	0	0	0	0	0	0	0		
2	301	4	358	1	0	0	0	85	267		
3	301	14	361	2	0	0	0	85	267		
4	301	14	358	3	0	0	0	85	267		
5	351	14	546	1	71	111	0	0	159		
6	0	4	0	0	0	0	0	0	0		
3 NOR DEL		2140	6	1500	101422		0	31013	101066		0
1	0	0	0	0	0	0	0	0	0		
2	300	4	358	1	0	0	0	85	267		
3	300	14	361	2	0	0	0	85	267		
4	300	14	358	3	0	0	0	85	267		
5	350	14	509	1	71	111	0	0	140		
6	0	4	0	0	0	0	0	0	0		
4 NOR		2150	7	61615	30666		0	61612		66	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	291	1	0	0	0	58	203		
3	201	14	288	2	0	0	0	58	203		
4	201	14	288	3	0	0	0	58	203		
5	251	14	461	1	73	106	0	0	461		
6	201	14	291	4	0	0	0	58	203		
7	0	4	0	0	0	0	0	0	0		
4 NOR		2160	7	61615	30666		0	61612		66	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	291	1	0	0	0	58	203		
3	200	14	288	2	0	0	0	58	203		
4	200	14	288	3	0	0	0	58	203		
5	250	14	436	1	73	106	0	0	436		
6	200	14	291	4	0	0	0	58	203		
7	0	4	0	0	0	0	0	0	0		
2 NAND		2190	5	41214	121666		0	21002		666	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	474	2	0	0	0	116	324		
3	211	14	471	1	0	0	0	122	344		
4	251	14	334	1	73	106	0	0	334		
5	0	4	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

2 NAND		2200	5	41214	121666		0	21002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	474	2	0	0	0	116	324		
3	210	14	471	1	0	0	0	122	344		
4	250	14	312	1	73	106	0	0	312		
5	0	4	0	0	0	0	0	0	0		
2 NAND DEL		2210	5	131613	111210		0	120002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	6	660	2	0	0	0	170	449		
3	311	16	658	1	0	0	0	180	479		
4	351	15	374	1	71	111	0	0	161		
5	0	5	0	0	0	0	0	0	0		
2 NAND DEL		2220	5	131613	111220		0	120002		666	0
1	0	0	0	0	0	0	0	0	0		
2	300	6	660	2	0	0	0	170	449		
3	310	16	658	1	0	0	0	180	479		
4	350	15	337	1	71	111	0	0	142		
5	0	5	0	0	0	0	0	0	0		
3 AND NOR		2230	6	61616	161666		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	474	2	0	0	0	116	324		
3	211	14	471	1	0	0	0	122	344		
4	203	14	273	3	0	0	0	58	192		
5	251	14	337	1	73	106	0	0	337		
6	0	4	0	0	0	0	0	0	0		
3 AND NOR		2240	6	61616	161666		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	474	2	0	0	0	116	324		
3	210	14	471	1	0	0	0	122	344		
4	202	14	273	3	0	0	0	58	192		
5	250	14	314	1	73	106	0	0	314		
6	0	4	0	0	0	0	0	0	0		
3 AND NOR DEL		2250	6	1310	101010		0	21002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	630	2	0	0	0	160	431		
3	311	14	620	1	0	0	0	169	445		
4	303	14	383	3	0	0	0	112	280		
5	351	14	406	1	71	111	0	0	51		
6	0	4	0	0	0	0	0	0	0		

3 AND NOR DEL		2260	6	1310	101020		0	21002		666	0
1	0	0	0	0	0	0	0	0	0		
2	300	4	630	2	0	0	0	160	431		
3	310	14	620	1	0	0	0	169	445		
4	302	14	383	3	0	0	0	112	280		
5	350	14	378	1	71	111	0	0	91		
6	0	4	0	0	0	0	0	0	0		
4 NAND OR		2270	7	60506	50666		0	60506	50666		0
1	0	0	0	0	0	0	0	0	0		
2	201	4	455	2	0	0	0	109	312		
3	211	14	452	1	0	0	0	115	328		
4	251	14	333	1	73	106	0	0	333		
5	213	14	452	3	0	0	0	115	328		
6	203	14	455	4	0	0	0	109	312		
7	0	4	0	0	0	0	0	0	0		
4 NAND OR		2280	7	60506	50666		0	60506	50666		0
1	0	0	0	0	0	0	0	0	0		
2	200	4	455	2	0	0	0	109	312		
3	210	14	452	1	0	0	0	115	328		
4	250	14	308	1	73	106	0	0	308		
5	212	14	452	3	0	0	0	115	328		
6	202	14	455	4	0	0	0	109	312		
7	0	4	0	0	0	0	0	0	0		
4 AND NOR		2290	7	60416	41666		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	458	2	0	0	0	109	309		
3	211	14	463	1	0	0	0	115	328		
4	203	14	281	3	0	0	0	58	195		
5	203	14	278	4	0	0	0	58	191		
6	251	14	445	1	73	106	0	0	445		
7	0	4	0	0	0	0	0	0	0		
4 AND NOR		2300	7	60416	41666		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	452	2	0	0	0	109	309		
3	210	14	457	1	0	0	0	115	328		
4	202	14	276	3	0	0	0	58	195		
5	202	14	272	4	0	0	0	58	191		
6	250	14	420	1	73	106	0	0	420		
7	0	4	0	0	0	0	0	0	0		

4 AND NOR DEL		2310	7	1310	101010		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	641	2	0	0	0	163	432		
3	311	14	638	1	0	0	0	173	453		
4	303	14	376	3	0	0	0	85	257		
5	303	14	367	4	0	0	0	85	255		
6	351	14	390	1	71	111	0	0	51		
7	0	4	0	0	0	0	0	0	0		
4 AND NOR DEL		2320	7	1310	101020		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	300	4	641	2	0	0	0	163	432		
3	310	14	638	1	0	0	0	173	453		
4	302	14	373	3	0	0	0	85	257		
5	302	14	372	4	0	0	0	85	255		
6	350	14	373	1	71	111	0	0	51		
7	0	4	0	0	0	0	0	0	0		
3 OR NAND		2330	6	61016	101012		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	441	2	0	0	0	109	303		
3	211	14	441	3	0	0	0	109	303		
4	251	14	480	1	73	106	0	0	480		
5	201	14	496	1	0	0	0	95	330		
6	0	4	0	0	0	0	0	0	0		
3 OR NAND		2340	6	61016	101022		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	441	2	0	0	0	109	303		
3	210	14	441	3	0	0	0	109	303		
4	250	14	448	1	73	106	0	0	448		
5	200	14	496	1	0	0	0	95	330		
6	0	4	0	0	0	0	0	0	0		
3 DATA SW		2350	6	61410	121666		0	1010	101013		0
1	0	0	0	0	0	0	0	0	0		
2	601	4	598	3	40	0	565	146	405		
3	403	14	192	2	40	0	565	37	137		
4	211	14	442	1	0	0	0	109	303		
5	451	14	369	1	73	106	0	0	369		
6	0	4	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

3 DATA SW		2360	6	61410	120666		0	1010	101020	0
1	0	0	0	0	0	0	0	0	0	
2	600	4	598	3	40	0	541	146	405	
3	402	14	192	2	40	0	541	37	137	
4	210	14	442	1	0	0	0	109	303	
5	450	14	345	1	73	106	0	0	345	
6	0	4	0	0	0	0	0	0	0	
DR 1 0		2370	5	621012	101010		0	21015	101051	0
1	0	0	0	0	0	0	0	0	0	
2	502	4	452	1	93	108	0	112	310	
3	352	14	707	2	93	108	0	0	360	
4	551	18	204	1	71	111	0	0	51	
5	0	10	0	0	0	0	0	0	0	
DR 1 0		2380	5	621012	101022		0	21015	101052	0
1	0	0	0	0	0	0	0	0	0	
2	501	4	452	1	93	108	0	112	310	
3	351	14	747	2	93	108	0	0	360	
4	550	18	196	1	71	111	0	0	51	
5	0	10	0	0	0	0	0	0	0	
DR 1 S		2390	5	621612	101010		0	21015	101051	0
1	0	0	0	0	0	0	0	0	0	
2	500	4	262	1	34	0	716	54	185	
3	500	14	260	3	34	0	716	37	171	
4	551	19	208	1	71	111	0	0	51	
5	0	12	0	0	0	0	0	0	0	
DR 1 S		2400	5	621612	101026		0	21015	101052	0
1	0	0	0	0	0	0	0	0	0	
2	501	4	262	1	34	0	742	54	185	
3	501	14	260	3	74	0	742	37	171	
4	550	19	209	1	71	111	0	0	51	
5	0	12	0	0	0	0	0	0	0	
DR 1 R		2410	5	311011	101010		0	21015	101050	0
1	0	0	0	0	0	0	0	0	0	
2	500	4	262	1	34	0	639	54	183	
3	301	14	394	4	0	0	0	75	259	
4	551	25	404	1	71	111	0	0	51	
5	0	7	0	0	0	0	0	0	0	

DR 1 R		2420	5	311011	101026		0	21015	101050		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	262	1	34	0	677	54	183		
3	300	14	394	4	0	0	0	75	259		
4	550	25	404	1	71	111	0	0	51		
5	0	7	0	0	0	0	0	0	0		
SR 1 S		2440	6	1010	101020		0	11002	52		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	225	3	34	0	705	44	173		
3	711	14	446	2	34	0	705	85	322		
4	503	14	356	1	34	0	705	0	256		
5	750	31	570	1	71	111	0	0	60		
6	0	5	0	0	0	0	0	0	0		
SR 1 0		2460	6	1210	101020		0	20002	666		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	907	1	0	0	0	0	627		
3	711	50	999	2	0	0	0	235	695		
4	351	14	915	2	93	108	0	0	506		
5	750	14	617	1	71	111	0	0	55		
6	0	4	0	0	0	0	0	0	0		
SR 1 0 R		2480	7	60316	60666		0	20002	24		0
1	0	0	0	0	0	0	0	0	0		
2	501	5	935	1	0	0	0	0	647		
3	711	32	1029	2	0	0	0	252	709		
4	300	39	371	4	0	0	0	75	267		
5	351	14	947	2	93	108	0	0	495		
6	750	14	837	1	71	111	0	0	120		
7	0	4	0	0	0	0	0	0	0		
SR 1 0 S K		2500	7	1310	101020		0	20002	220		0
1	0	0	0	0	0	0	0	0	0		
2	501	5	906	1	0	0	0	0	626		
3	719	62	1176	2	0	0	0	235	864		
4	503	14	488	3	0	0	0	112	356		
5	351	14	1207	2	93	108	0	0	562		
6	750	14	742	1	71	111	0	0	67		
7	0	4	0	0	0	0	0	0	0		

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DUAL SR		2520	8	1500	101022		0	21012	101026	0
1	0	0	0	0	0	0	0	0	0	
2	711	5	1106	2	0	0	0	248	814	
3	501	16	900	1	0	0	0	0	620	
4	503	16	962	3	0	0	0	0	662	
5	713	59	1027	4	0	0	0	262	735	
6	351	21	1571	2	93	108	0	0	573	
7	750	14	765	1	71	111	0	0	168	
8	0	4	0	0	0	0	0	0	0	
SCHMITT		2560	4	11612	101022		0	11011	101012	0
1	0	0	0	0	0	0	0	0	0	
2	501	4	1012	1	100	0	10	194	589	
3	550	70	134	1	71	111	0	0	63	
4	0	4	0	0	0	0	0	0	0	
SCHMITT		2570	4	11612	101012		0	11011	101022	0
1	0	0	0	0	0	0	0	0	0	
2	501	4	1012	1	100	0	10	194	589	
3	550	70	134	1	71	111	0	0	63	
4	0	4	0	0	0	0	0	0	0	
DR 1		2580	4	341614	121024		0	21010	101056	0
1	0	0	0	0	0	0	0	0	0	
2	501	4	251	1	34	0	412	54	177	
3	550	35	310	1	71	111	0	0	160	
4	0	7	0	0	0	0	0	0	0	
SR 1		2600	5	101010	101020		0	31013	101052	0
1	0	0	0	0	0	0	0	0	0	
2	711	5	445	2	34	0	633	85	321	
3	501	16	384	1	34	0	633	0	276	
4	750	39	427	1	71	111	0	0	59	
5	0	5	0	0	0	0	0	0	0	
SR 1 R		2620	6	11011	101021		0	31013	101052	0
1	0	0	0	0	0	0	0	0	0	
2	711	5	443	2	34	0	677	85	319	
3	501	16	384	1	34	0	677	0	276	
4	300	15	346	4	0	0	0	82	250	
5	750	28	539	1	71	111	0	0	60	
6	0	4	0	0	0	0	0	0	0	

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SR 1 0 S		2640	7	1310	101020		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	899	1	0	0	0	0	619		
3	711	54	1012	2	0	0	0	238	700		
4	503	14	488	3	0	0	0	112	356		
5	351	14	1188	2	93	108	0	0	556		
6	750	14	726	1	71	111	0	0	71		
7	0	4	0	0	0	0	0	0	0		
SR 1 0 K		2660	6	111011	101020		0	20002		21	0
1	0	0	0	0	0	0	0	0	0		
2	501	5	900	1	0	0	0	0	620		
3	719	53	1223	2	0	0	0	244	939		
4	351	17	1111	2	93	108	0	0	571		
5	750	19	642	1	71	111	0	0	100		
6	0	5	0	0	0	0	0	0	0		
SR 1 0 R K		2680	7	60316	60666		0	20002		24	0
1	0	0	0	0	0	0	0	0	0		
2	501	5	935	1	0	0	0	0	647		
3	719	32	1237	2	0	0	0	252	917		
4	300	39	371	4	0	0	0	71	267		
5	351	14	947	2	93	108	0	0	495		
6	750	14	837	1	71	111	0	0	120		
7	0	4	0	0	0	0	0	0	0		
BINARY		2700	6	631213	121220		0	620002		51	0
1	0	0	0	0	0	0	0	0	0		
2	2101	12	875	1	34	0	691	194	619		
3	750	44	1055	3	93	108	0	0	645		
4	1151	33	881	2	93	108	0	0	370		
5	1750	14	357	1	71	111	0	0	192		
6	0	17	0	0	0	0	0	0	0		
DUAL SR 1		2720	7	201213	111123		0	21012	101056		0
1	0	0	0	0	0	0	0	0	0		
2	711	5	601	2	36	0	1219	82	485		
3	501	16	359	1	36	0	1219	0	263		
4	503	16	364	3	36	0	1219	0	268		
5	713	16	472	4	36	0	1219	82	356		
6	750	40	561	1	71	111	0	0	59		
7	0	6	0	0	0	0	0	0	0		

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INV		4010	4	11016	141416		0	21002		66	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	458	1	0	0	0	109	314		
3	251	14	291	1	143	122	0	0	291		
4	0	4	0	0	0	0	0	0	0		
INV		4020	4	11016	141426		0	21002		66	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	458	1	0	0	0	109	314		
3	250	14	269	1	143	122	0	0	269		
4	0	4	0	0	0	0	0	0	0		
INV DEL		4050	4	251212	101010		0	620002		656	0
1	0	0	0	0	0	0	0	0	0		
2	301	10	618	1	0	0	0	160	422		
3	351	14	281	1	143	127	0	0	85		
4	0	6	0	0	0	0	0	0	0		
INV DEL		4060	4	251212	101026		0	620002		656	0
1	0	0	0	0	0	0	0	0	0		
2	300	10	618	1	0	0	0	160	422		
3	350	14	253	1	143	127	0	0	85		
4	0	6	0	0	0	0	0	0	0		
2 NOR		4070	5	40204	20616		0	20002		266	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	458	1	0	0	0	109	314		
3	251	14	347	1	143	122	0	0	347		
4	201	14	458	2	0	0	0	109	314		
5	0	4	0	0	0	0	0	0	0		
2 NOR		4080	5	40204	20626		0	20002		266	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	458	1	0	0	0	109	314		
3	250	14	325	1	143	122	0	0	325		
4	200	14	458	2	0	0	0	109	314		
5	0	4	0	0	0	0	0	0	0		
2 NOR DEL		4090	5	521612	101216		0	21002		452	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	622	1	0	0	0	160	423		
3	301	14	619	2	0	0	0	160	423		
4	351	14	524	1	143	127	0	0	229		
5	0	9	0	0	0	0	0	0	0		

2 NOR DEL		4100	5	521612	101026		0	21002		452	0
1	0	0	0	0	0	0	0	0	0		
2	300	4	622	1	0	0	0	160	423		
3	300	14	619	2	0	0	0	160	423		
4	350	14	489	1	143	127	0	0	215		
5	0	9	0	0	0	0	0	0	0		
3 NOR		4110	6	41316	131626		0	21002		266	0
1	0	0	0	0	0	0	0	0	0		
2	201	4	458	1	0	0	0	109	317		
3	201	14	458	2	0	0	0	109	317		
4	201	14	456	3	0	0	0	109	317		
5	251	14	575	1	143	122	0	0	575		
6	0	4	0	0	0	0	0	0	0		
3 NOR		4120	6	41316	131626		0	21002		266	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	458	1	0	0	0	109	317		
3	200	14	458	2	0	0	0	109	317		
4	200	14	456	3	0	0	0	109	317		
5	250	14	553	1	143	122	0	0	553		
6	0	4	0	0	0	0	0	0	0		
3 NOR DEL		4130	6	621612	101316		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	624	1	0	0	0	160	425		
3	301	14	622	2	0	0	0	160	425		
4	301	14	624	3	0	0	0	160	425		
5	351	14	708	1	143	127	0	0	209		
6	0	11	0	0	0	0	0	0	0		
3 NOR DEL		4140	6	621612	101326		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	300	4	624	1	0	0	0	160	425		
3	300	14	622	2	0	0	0	160	425		
4	300	14	624	3	0	0	0	160	425		
5	350	14	645	1	143	127	0	0	190		
6	0	11	0	0	0	0	0	0	0		

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4	NOR		4150	7	11305	30666		0	11002	666	0
	1	0	0	0	0	0	0	0	0		
	2	201	4	444	1	0	0	0	109	305	
	3	201	14	444	2	0	0	0	109	315	
	4	201	14	444	3	0	0	0	109	305	
	5	251	14	666	1	143	122	0	0	666	
	6	201	14	444	4	0	0	0	109	308	
	7	0	4	0	0	0	0	0	0	0	
4	NOR		4160	7	11305	31666		0	11002	666	0
	1	0	0	0	0	0	0	0	0	0	
	2	200	4	444	1	0	0	0	109	305	
	3	200	14	444	2	0	0	0	109	315	
	4	200	14	444	3	0	0	0	109	305	
	5	250	14	649	1	143	122	0	0	649	
	6	200	14	444	4	0	0	0	109	308	
	7	0	4	0	0	0	0	0	0	0	
4	NOR DEL		4170	7	421612	101666		0	11002	666	0
	1	0	0	0	0	0	0	0	0	0	
	2	301	4	624	1	0	0	0	160	425	
	3	301	14	622	2	0	0	0	160	425	
	4	301	14	624	3	0	0	0	160	425	
	5	301	14	622	4	0	0	0	160	421	
	6	351	14	778	1	143	122	0	0	224	
	7	0	8	0	0	0	0	0	0	0	
4	NOR DEL		4180	7	421612	101666		0	11002	666	0
	1	0	0	0	0	0	0	0	0	0	
	2	300	4	624	1	0	0	0	160	425	
	3	300	14	622	2	0	0	0	160	425	
	4	300	14	624	3	0	0	0	160	425	
	5	300	14	622	4	0	0	0	160	421	
	6	350	14	721	1	143	127	0	0	295	
	7	0	8	0	0	0	0	0	0	0	
2	NAND		4190	5	621012	101666		0	11002	666	0
	1	0	0	0	0	0	0	0	0	0	
	2	201	4	924	2	0	0	0	245	625	
	3	211	14	920	1	0	0	0	259	655	
	4	251	14	507	1	143	122	0	0	507	
	5	0	13	0	0	0	0	0	0	0	

2 NAND		4200	5	621012	101666		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	4	924	2	0	0	0	245	625		
3	210	14	920	1	0	0	0	259	655		
4	250	14	473	1	143	122	0	0	473		
5	0	13	0	0	0	0	0	0	0		
2 NAND DEL		4210	5	611611	101614		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	1284	2	0	0	0	347	865		
3	311	14	1280	1	0	0	0	367	807		
4	351	38	674	1	143	127	0	0	186		
5	0	10	0	0	0	0	0	0	0		
2 NAND DEL		4220	5	611611	101624		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	300	4	1280	2	0	0	0	347	865		
3	310	14	1280	1	0	0	0	367	807		
4	350	38	660	1	143	127	0	0	171		
5	0	10	0	0	0	0	0	0	0		
3 AND NOR		4230	6	420002	666		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	201	5	941	2	0	0	0	248	660		
3	211	16	936	1	0	0	0	263	666		
4	251	16	640	1	143	122	0	0	640		
5	203	16	447	3	0	0	0	109	319		
6	0	9	0	0	0	0	0	0	0		
3 AND NOR		4240	6	420002	666		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	200	5	941	2	0	0	0	248	660		
3	210	16	936	1	0	0	0	263	666		
4	250	16	596	1	143	122	0	0	596		
5	202	16	447	3	0	0	0	109	319		
6	0	9	0	0	0	0	0	0	0		
3 AND NOR DEL		4250	6	21612	101316		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	301	4	1308	2	0	0	0	354	881		
3	311	14	1259	1	0	0	0	382	896		
4	303	50	618	3	0	0	0	160	413		
5	351	14	973	1	143	127	0	0	262		
6	0	4	0	0	0	0	0	0	0		

3 AND NOR DEL		4260	6	21612	101326		0	11002	666		0
1	0	0	0	0	0	0	0	0	0		
2	300	4	1308	2	0	0	0	354	881		
3	310	14	1259	1	0	0	0	382	896		
4	302	50	618	3	0	0	0	160	413		
5	350	14	908	1	143	127	0	0	239		
6	0	4	0	0	0	0	0	0	0		
DATA SW		4350	6	41012	101226		0	1010	1666		0
1	0	0	0	0	0	0	0	0	0		
2	601	4	1054	3	34	0	787	241	631		
3	403	14	192	2	34	0	787	37	137		
4	211	14	822	1	0	0	0	227	588		
5	451	23	496	1	143	122	0	0	496		
6	0	5	0	0	0	0	0	0	0		
DATA SW		4360	6	41012	101226		0	1010	1666		0
1	0	0	0	0	0	0	0	0	0		
2	600	4	1054	3	34	0	766	241	631		
3	402	14	192	2	34	0	766	37	137		
4	210	14	822	1	0	0	0	227	588		
5	450	23	468	1	143	122	0	0	468		
6	0	5	0	0	0	0	0	0	0		
DR 1 0		4370	5	201010	101011		0	1010	101050		0
1	0	0	0	0	0	0	0	0	0		
2	500	4	748	1	0	0	0	214	520		
3	350	36	1235	2	165	125	0	0	530		
4	551	14	429	1	143	127	0	0	74		
5	0	8	0	0	0	0	0	0	0		
DR 1 0		4380	5	201010	101021		0	1010	101050		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	747	1	0	0	0	214	520		
3	351	36	1270	2	165	125	0	0	530		
4	550	15	400	1	143	127	0	0	74		
5	0	7	0	0	0	0	0	0	0		
DR 1 S		4390	5	621012	101010		0	21015	101050		0
1	0	0	0	0	0	0	0	0	0		
2	500	4	262	1	34	0	1023	54	186		
3	500	14	260	3	34	0	1023	37	170		
4	551	22	378	1	143	127	0	0	68		
5	0	12	0	0	0	0	0	0	0		

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DR 1 S		4400	5	621012	101026		0	21015	101052		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	262	1	34	0	1049	54	186		
3	501	14	260	3	34	0	1049	37	170		
4	550	22	378	1	143	127	0	0	68		
5	0	12	0	0	0	0	0	0	0		
DR 1 R		4410	5	201010	101010		0	1010	101052		0
1	0	0	0	0	0	0	0	0	0		
2	500	4	265	1	34	0	870	54	186		
3	301	14	688	4	0	0	0	156	456		
4	551	36	657	1	143	127	0	0	68		
5	0	8	0	0	0	0	0	0	0		
DR 1 R		4420	5	201010	101020		0	1010	101052		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	265	1	34	0	901	54	186		
3	300	14	688	4	0	0	0	156	456		
4	550	36	630	1	143	127	0	0	68		
5	0	8	0	0	0	0	0	0	0		
SR PH 2-1 R		4430	6	221611	101210		0	20002		52	0
1	0	0	0	0	0	0	0	0	0		
2	400	5	264	1	34	0	929	0	196		
3	610	16	354	2	34	0	929	58	262		
4	301	31	622	4	0	0	0	160	442		
5	751	19	704	1	143	125	0	0	211		
6	0	7	0	0	0	0	0	0	0		
SR 1 S		4440	6	111411	101021		0	20002		52	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	232	3	34	0	1038	48	176		
3	711	14	451	2	34	0	1038	85	327		
4	503	14	356	1	34	0	1038	0	256		
5	750	34	639	1	143	127	0	0	93		
6	0	5	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

SR PH2-1 0 1 R		4450	7	21612	101210		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	400	5	672	1	0	0	0	0	468		
3	610	16	784	2	0	0	0	173	552		
4	250	36	1045	2	93	108	0	0	1045		
5	301	16	625	4	0	0	0	160	437		
6	751	16	961	1	143	127	0	0	210		
7	0	5	0	0	0	0	0	0	0		
SR 1 0		4460	6	201010	101050		0	1002		666	0
1	0	0	0	0	0	0	0	0	0		
2	501	5	1516	1	0	0	0	0	1032		
3	711	16	1646	2	0	0	0	408	1166		
4	351	71	1468	2	165	125	0	0	827		
5	750	16	970	1	143	127	0	0	70		
6	0	7	0	0	0	0	0	0	0		
SR 1 0 R		4480	7	1010	101020		0	11002		666	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	1500	1	0	0	0	0	1024		
3	711	14	1633	2	0	0	0	428	1134		
4	300	84	658	4	0	0	0	150	462		
5	351	14	1555	2	165	125	0	0	806		
6	750	15	1043	1	143	127	0	0	83		
7	0	5	0	0	0	0	0	0	0		
SR 1 0 S K		4500	7	620000	222		0	20002		666	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	1499	1	0	0	0	0	1023		
3	719	14	1698	2	0	0	0	408	1194		
4	503	14	814	3	0	0	0	197	562		
5	351	85	1864	2	165	125	0	0	938		
6	750	29	1102	1	143	127	0	0	189		
7	0	11	0	0	0	0	0	0	0		
DUAL SR 1 0		4520	8	1210	101056		0	21012	101666		0
1	0	0	0	0	0	0	0	0	0		
2	711	4	1691	2	0	0	0	394	1199		
3	501	14	1421	1	0	0	0	0	965		
4	503	14	1498	3	0	0	0	0	1018		
5	713	14	1631	4	0	0	0	405	1123		
6	351	131	2646	2	165	125	0	0	849		
7	750	15	845	1	143	127	0	0	94		
8	0	4	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

RS FF		4530	6	10001		666	0	10001		666	0
1	0	0	0	0	0	0	0	0	0		
2	401	4	503	3	0	0	0	126	345		
3	251	15	935	2	198	130	0	0	935		
4	653	23	867	1	198	130	0	0	867		
5	203	15	503	4	0	0	0	126	343		
6	0	4	0	0	0	0	0	0	0		
RS FF		4540	6	10001		666	0	10001		666	0
1	0	0	0	0	0	0	0	0	0		
2	400	4	503	3	0	0	0	126	345		
3	250	15	882	2	198	130	0	0	882		
4	652	23	827	1	198	130	0	0	827		
5	202	15	501	4	0	0	0	126	343		
6	0	4	0	0	0	0	0	0	0		
DR 1		4580	4	21011	101026		0	21012	101051		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	257	1	34	0	837	54	182		
3	550	40	448	1	143	127	0	0	148		
4	0	4	0	0	0	0	0	0	0		
SR 1		4600	5	21012	101021		0	31013	101052		0
1	0	0	0	0	0	0	0	0	0		
2	711	5	443	2	34	0	946	84	319		
3	501	16	381	1	34	0	946	0	273		
4	750	40	569	1	143	127	0	0	91		
5	0	4	0	0	0	0	0	0	0		
SR 1 R		4620	6	1010	101020		0	31013	101052		0
1	0	0	0	0	0	0	0	0	0		
2	711	5	455	2	34	0	960	85	331		
3	501	16	428	1	34	0	960	0	308		
4	300	37	696	4	0	0	0	197	484		
5	750	14	704	1	143	127	0	0	99		
6	0	4	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

SR 1 0 S		4640	7	621612	101020		0	21002		666		0
1	0	0	0	0	0	0	0	0	0			
2	501	4	1500	1	0	0	0	0	1020			
3	711	14	1642	2	0	0	0	408	1134			
4	503	14	815	3	0	0	0	197	563			
5	351	84	1752	2	165	125	0	0	882			
6	750	15	977	1	143	127	0	0	92			
7	0	17	0	0	0	0	0	0	0			
SR 1 0 K		4660	6	61010	101020		0	21002		120		0
1	0	0	0	0	0	0	0	0	0			
2	501	4	1500	1	0	0	0	0	1020			
3	719	14	1856	2	0	0	0	449	1344			
4	351	89	1574	2	165	125	0	0	843			
5	750	14	838	1	143	127	0	0	132			
6	0	4	0	0	0	0	0	0	0			
SR 1 0 R K		4680	7	21012	101020		0	20002		210		0
1	0	0	0	0	0	0	0	0	0			
2	501	4	1500	1	0	0	0	0	1020			
3	719	14	1843	2	0	0	0	442	1339			
4	300	87	660	4	0	0	0	150	464			
5	351	21	1607	2	165	125	0	0	809			
6	750	14	1022	1	143	127	0	0	92			
7	0	4	0	0	0	0	0	0	0			
PROT DIODE		5020	3	30n215	61666		0	200214		60666		0
1	0	0	0	0	0	0	0	0	0			
2	2	6	254	1	0	0	0	0	254			
3	0	7	0	0	0	0	0	0	0			
PH 1 2 NOR		5030	5	621012	101666		0	621012		101666		0
1	0	0	0	0	0	0	0	0	0			
2	201	10	990	1	0	0	0	303	692			
3	251	27	914	1	320	152	0	0	914			
4	201	28	990	2	0	0	0	303	692			
5	0	10	0	0	0	0	0	0	0			
PH 2 2 NOR		5040	5	621012	101666		0	621012		101666		0
1	0	0	0	0	0	0	0	0	0			
2	200	10	990	1	0	0	0	303	692			
3	250	27	914	1	320	152	0	0	914			
4	200	28	990	2	0	0	0	303	692			
5	0	10	0	0	0	0	0	0	0			

CIRCUIT TYPE FILE JUNE 1969

PH 1 KILL		5090	3	31013	101213		0	620002	666		0
1	0	0	0	0	0	0	0	0	0		
2	6	14	171	1	100	0	0	0	171		
3	0	4	0	0	0	0	0	0	0		
P CG		6000	4	11012	1666		0	11016	121526		0
1	0	0	0	0	0	0	0	0	0		
2	100	4	205	1	0	0	0	0	180		
3	150	14	239	1	0	0	0	0	208		
4	0	4	0	0	0	0	0	0	0		
P CG		6010	4	11012	1666		0	11016	121515		0
1	0	0	0	0	0	0	0	0	0		
2	101	4	205	1	0	0	0	0	180		
3	151	14	239	1	0	0	0	0	208		
4	0	4	0	0	0	0	0	0	0		
CG		6020	4	11016	101666		0	11016	101666		0
1	0	0	0	0	0	0	0	0	0		
2	100	4	165	1	0	0	0	0	145		
3	150	14	165	1	0	0	0	0	143		
4	0	4	0	0	0	0	0	0	0		
CG		6030	4	11016	101666		0	11016	101666		0
1	0	0	0	0	0	0	0	0	0		
2	101	4	165	1	0	0	0	0	145		
3	151	14	165	1	0	0	0	0	143		
4	0	4	0	0	0	0	0	0	0		
PH 2 KILL		6040	3	31013	101226		0	620002	666		0
1	0	0	0	0	0	0	0	0	0		
2	7	14	171	1	100	0	0	0	171		
3	0	4	0	0	0	0	0	0	0		
SIGNAL KILL		6050	4	21012	101666		0	20002	666		0
1	0	0	0	0	0	0	0	0	0		
2	3	4	659	1	0	0	0	0	449		
3	8	16	265	2	100	0	0	0	265		
4	0	4	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

PUSH PULL BUF		6060	4	201010	101666		0	11012	101666		0
1	0	0	0	0	0	0	0	0	0		
2	200	4	2109	1	0	0	0	595	1416		
3	250	26	959	1	93	108	0	0	0		
4	0	49	0	0	0	0	0	0	0		
50 PCB		6070	4	431013	101056		0	21002		10	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	368	1	100	0	10	88	255		
3	475	47	676	1	93	108	0	0	0		
4	0	8	0	0	0	0	0	0	0		
50 PCB		6080	4	431013	101056		0	21002		20	0
1	0	0	0	0	0	0	0	0	0		
2	500	4	368	1	100	0	10	88	255		
3	475	47	657	1	93	108	0	0	0		
4	0	8	0	0	0	0	0	0	0		
75 PCB		6090	4	21012	101014		0	11002		12	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	444	1	100	0	10	109	305		
3	475	78	963	1	93	108	0	0	0		
4	0	4	0	0	0	0	0	0	0		
75 PCB		6100	4	21012	101024		0	11002		22	0
1	0	0	0	0	0	0	0	0	0		
2	500	4	444	1	100	0	10	109	305		
3	475	78	921	1	93	108	0	0	0		
4	0	4	0	0	0	0	0	0	0		
100 PCB		6110	4	621012	101356		0	20000		666	0
1	0	0	0	0	0	0	0	0	0		
2	501	4	579	1	100	0	10	150	399		
3	475	70	1144	1	93	108	0	0	0		
4	0	29	0	0	0	0	0	0	0		
100 PCB		6120	4	621012	101356		0	20000		666	0
1	0	0	0	0	0	0	0	0	0		
2	500	4	569	1	100	0	10	150	399		
3	475	70	1127	1	90	108	0	0	0		
4	0	29	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

SR START		6140	5	660606	60666		0	20002	51		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	276	1	0	0	392	0	0		
3	503	14	377	2	0	0	392	82	259		
4	574	14	449	1	0	0	0	0	0		
5	0	33	0	0	0	0	0	0	0		
SR MIDDLE		6160	5	660606	60666		0	660606	60666		0
1	0	0	0	0	0	0	0	0	0		
2	523	4	229	1	0	0	397	0	0		
3	574	14	340	2	0	0	397	0	0		
4	574	14	440	1	0	0	0	0	0		
5	0	32	0	0	0	0	0	0	0		
SR END		6180	5	1510	101326		0	660606	60666		0
1	0	0	0	0	0	0	0	0	0		
2	523	18	229	1	0	0	432	0	0		
3	574	14	294	2	0	0	432	0	0		
4	552	26	442	1	27	0	0	0	155		
5	0	4	0	0	0	0	0	0	0		
DR START		6200	4	660606	60666		0	21010	101056		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	244	1	0	0	254	54	194		
3	574	14	60	1	0	0	0	0	0		
4	0	25	0	0	0	0	0	0	0		
DR MIDDLE		6220	4	660606	60666		0	660606	60666		0
1	0	0	0	0	0	0	0	0	0		
2	523	4	116	1	0	0	239	0	0		
3	574	14	125	1	0	0	0	0	0		
4	0	30	0	0	0	0	0	0	0		
DR END		6240	4	600610	61626		0	660606	60666		0
1	0	0	0	0	0	0	0	0	0		
2	523	4	116	1	0	0	277	0	0		
3	552	39	210	1	27	0	0	0	135		
4	0	11	0	0	0	0	0	0	0		
10 INV		6250	4	621012	101655		0	21012	101666		0
1	0	0	0	0	0	0	0	0	0		
2	201	4	1098	1	0	0	0	333	759		
3	251	15	595	1	386	193	0	0	595		
4	0	22	0	0	0	0	0	0	0		

CIRCUIT TYPE FILE JUNE 1969

10 INV		6260	4	621012	101655		0	21012	101666		0
1	0	0	0	0	0	0	0	0	0		
2	200	4	1098	1	0	0	0	333	799		
3	250	15	563	1	386	163	0	0	563		
4	0	22	0	0	0	0	0	0	0		
PH N CG		6270	5	61516	161666		0	61516	161666		0
1	0	0	0	0	0	0	0	0	0		
2	25	4	133	1	0	0	0	0	95		
3	28	14	200	2	0	0	0	41	143		
4	8	14	133	1	0	0	0	0	95		
5	0	4	0	0	0	0	0	0	0		
PH N PCG		6280	5	61516	161666		0	61516	151666		0
1	0	0	0	0	0	0	0	0	0		
2	25	4	272	1	0	0	0	0	235		
3	28	14	200	2	0	0	0	41	143		
4	8	14	133	1	0	0	0	0	115		
5	0	4	0	0	0	0	0	0	0		
30 PCA		6290	4	561612	101052		0	20002	11		0
1	0	0	0	0	0	0	0	0	0		
2	501	4	296	1	100	0	637	68	207		
3	475	41	505	1	93	108	0	0	346		
4	0	9	0	0	0	0	0	0	0		
30 PCB		6300	4	561612	101052		0	20002	11		0
1	0	0	0	0	0	0	0	0	0		
2	500	4	296	1	100	0	621	68	207		
3	475	41	488	1	93	108	0	0	329		
4	0	9	0	0	0	0	0	0	0		
DR DUMMY		8500	4	600000	56		0	600000	666		0
1	0	0	0	0	0	0	0	0	0		
2	501	14	300	1	0	0	0	0	0		
3	550	14	300	1	0	0	0	0	0		
4	0	20	0	0	0	0	0	0	0		
PAD		9034	3	0	0		0	0	0		0
1	0	0	0	0	0	0	0	0	0		
2	4	20	346	1	0	0	0	0	0		
3	0	20	0	0	0	0	0	0	0		

Appendix A

DESIGN PROCEDURE FOR A MOS-FET DIGITAL BUILDING BLOCK FAMILY

MOS digital building blocks or "standard cells" can be reduced to three basic MOS circuits: the MOS inverter, the MOS inverter with coupling device, and the NAND configuration or "series stack". The following design procedure used for the basic inverter will be extended to include the other two basic configurations. A few preliminary comments should be made before listing the initial assumptions that were made for this design procedure.

The design is accomplished with the aid of a computer program written around the saturated and nonsaturated device equations derived from the physical model of C. T. Sah. The Sah model represents a reasonably accurate description of the MOS transistor in both regions of operation, saturated and nonsaturated. Previous design approaches assumed negligible turn-on time of the bottom inverter device provided a sufficiently large One-level was present at the gate of the device. This assumption is no longer necessary since the computer can economically calculate and present the large number of points necessary for the complete solution of the equations. The computer also allows a wide expansion of the number of worst cases that can easily be simulated. The analysis also provides typical on-chip signal waveforms rather than step-function signal inputs.

The following equations are derived from the Sah model and describe the saturated and nonsaturated regions of operation of the MOS device:

Nonsaturated: $$I_{DS} = K\left[2(V_{GS} - V_T)\, V_{DS} - V_{DS}^2\right] \; ; \text{for } V_{GS} - V_T \geq V_{DS} \qquad \text{(A-1)}$$

Saturated: $$I_{DS} = K\,(V_{IN} - V_T)^2 \; ; \quad \text{for } V_{GS} - V_T \leq V_{DS} \qquad \text{(A-2)}$$

$$I_{DS} = 0 \; ; \quad \text{for } V_{GS} - V_T \leq 0 \qquad \text{(A-3)}$$

Body Effect Correction: $V_T' = V_T + .5\sqrt{V_{BS}}$ (A-4)

Figure A-1 shows a typical MOS inverter.

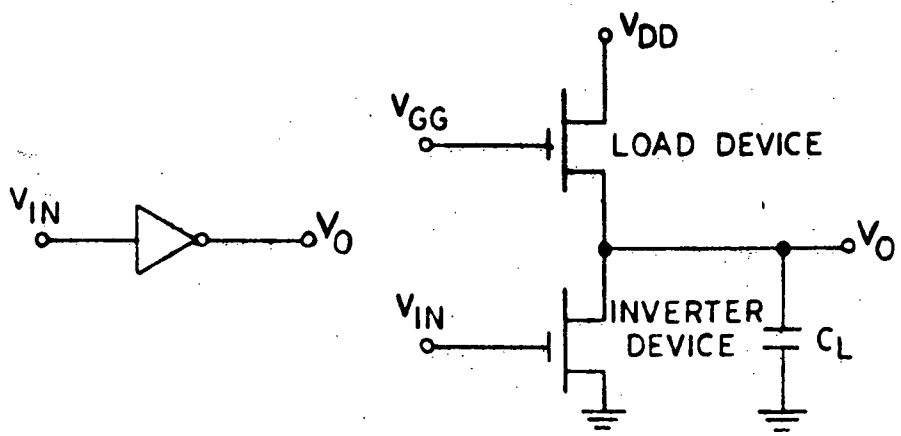

Fig. A-1. Typical MOS inverter.

The building block family has been designed for a four-level propagation delay capability during each of two clock phases. During the time the V_{GG} clock pulse is present the load device will be in the nonsaturated condition and the current through the load device can be obtained from equation (A-1):

$$I_{DS} = K_L \left[2(V_{GG} - V_T' - V_0)(V_{DD} - V_0) - (V_{DD} - V_0)^2\right] \quad (A-5)$$

equation (A-5) when expanded becomes:

$$I_{DS} = K_L \left[2(V_{GG} - V_T')V_{DD} - V_{DD}^2 - 2(V_{GG} - V_T')V_0 + V_0^2\right] \quad (A-6)$$

where $V_T' = V_T + .5\sqrt{V_0}$

Both equations (A-1) and (A-2) are required to describe the current through the inverter device because both the saturated and the nonsaturated regions occur during the traverse from logical Zero to logical One of the input voltage V_{IN}.

The inverter device current becomes:

Nonsaturated: $$I_{DS} = K_I \left[2(V_{IN} - V_T)\ V_0 - V_0^2 \right] \quad \text{for } V_{IN} - V_T > V_0 \qquad (A\text{-}7)$$

Saturated: $$I_{DS} = K_I\ (V_{IN} - V_T)^2 \quad \text{for } V_{IN} - V_T \leq V_0 \qquad (A\text{-}8)$$

The K of a device can be related to its physical dimensions by the equation

$$K = K' \frac{W}{\ell},$$

where K' = the processing constant: $\dfrac{\mu_p \epsilon_{ox}}{2\, t_{ox}}$

W = the width of the thin-oxide gate region
ℓ = the length of the inverter channel after diffusion

As each point of the inverter output waveform is calculated, the computer program tests for saturated or nonsaturated conditions of the bottom device operation and automatically selects either equation (A-7) or (A-8).

By cascading four inverter devices to form an inverter chain, it is possible to use the program to analyze the worst-case response of the four-delay logic system shown in Fig. A-2.

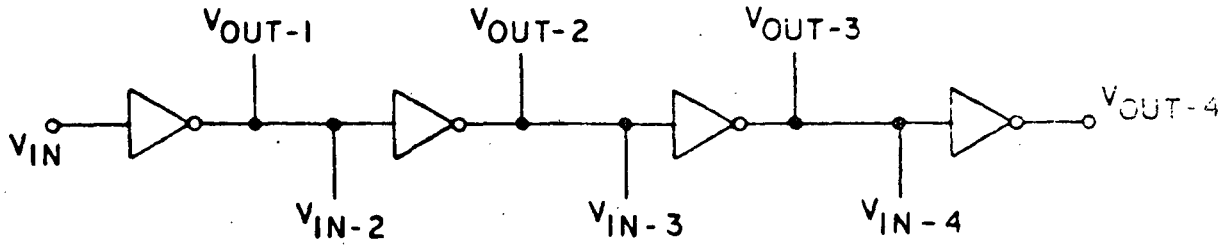

Fig. A-2. Four-delay logic system.

It is practical to assume that initial conditions were established at each node during the previous clocking interval. For a two-phase clocked system, however, V_{IN} will be established at the opposite clock phase and presented to the input of the inverter chain prior to the clocking interval of the inverter chain. For this analysis, at t = 0, the clock waveform turns on to V_{GG}. As shown in Fig. A-2, the input voltage of each of the remaining inverters is equal to the output voltage of its predecessor.

The instantaneous output voltage of any node may be expressed as follows:

$$V_0 \text{ (at time t)} = V_0 \text{ (at time t - } \Delta t) + \Delta V_0 \tag{A-9}$$

$$\text{where } \Delta V_0 = (I_0/C_L)\ \Delta t \tag{A-10}$$

$$\text{and } I_0 = I_L - I_I \text{ (see Fig. A-3)} \tag{A-11}$$

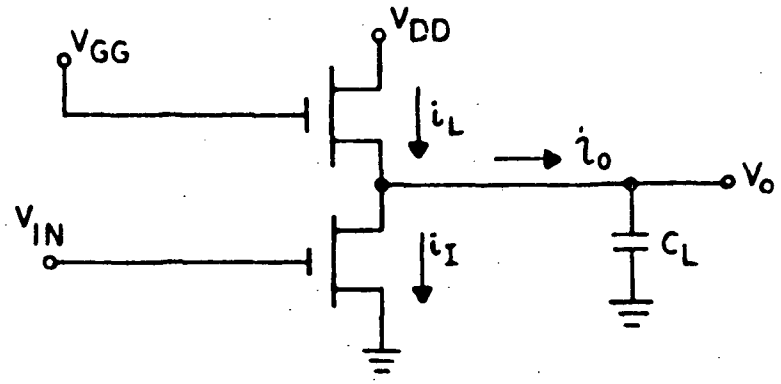

Fig. A-3. Representation of I_0.

I_L is calculated using equation (A-6). I_I is calculated using equations (A-7) and (A-8), depending upon the operating region of the inverter device as previously defined. These currents are calculated for time (t) using values of V_0, V_T', and V_{IN} obtained at time (t - Δt). I_0 can then be calculated from equation (A-11) and a new value of V_0 is obtained from equation (A-10). The value of Δt used in equation (A-10) must be chosen small enough to permit an assumption of constant-current between time (t - Δt) and time (t) to

to be made. The degree of precision desired for each Δv is also important. It has been found that $\Delta t = .5$ nanoseconds gives results correct to the nearest .02 volt, which is more than adequate for this analysis. The calculations are thus repeated as many times as necessary until the desired end-point is established.

When applying this analysis to an actual circuit design, R_{SC}, or the short circuit resistance of the load device, is considered first and is given by the equation

$$R_{SC} = \frac{1}{K_L \left[2 (V_{GG} - V_T) - V_{DD}\right]} \qquad \text{where } K_L = K' \frac{W}{\ell} \tag{A-12}$$

By combining equations (A-9) and (A-10)

$$V_0 \text{ (at time t)} = V_0 \left[at (t - \Delta t)\right] + \frac{I_0}{C_L} \Delta t$$

$$= V_0 \left[at (t - \Delta t)\right] + I_0 R_{SC} \frac{\Delta t}{R_{SC} C_L}$$

By substituting $\tau = R_{SC} C_L$,

$$V_0 (t) = V_0 (t - \Delta t) + I_0 R_{SC} \frac{(\Delta t)}{(\tau)} \tag{A-13}$$

and multiplying equation (A-11) by R_{SC}

$$I_0 R_{SC} = I_L R_{SC} - I_I R_{SC}, \text{ and}$$

$$I_L R_{SC} = \frac{2(V_{GG} - V'_T) V_{DD} - V_{DD}^2 - 2 (V_{GG} - V'_T) V_0 + V_0^2}{2(V_{GG} - V_T) - V_{DD}} \tag{A-14}$$

$$I_I R_{SC} = \frac{\frac{K_I}{K_L}\left[(V_{IN} - V_T)^2\right]}{2(V_{GG} - V_T) - V_{DD}} \quad \text{for} \quad V_{IN} - V_T \leq V_0 \tag{A-15}$$

and

$$I_I R_{SC} = \frac{\frac{K_I}{K_L}\left[2\,(V_{IN} - V_T)\,V_0 - V_0^2\right]}{2(V_{GG} - V_T) - V_{DD}} \quad \text{for } V_{IN} - V_T \geq V_0 \tag{A-16}$$

Since the logic system requires the capability to propagate through four levels of logic in one clock time, the following worst-case initial conditions are assumed for a typical four-delay inverter chain shown in Fig. A-4.

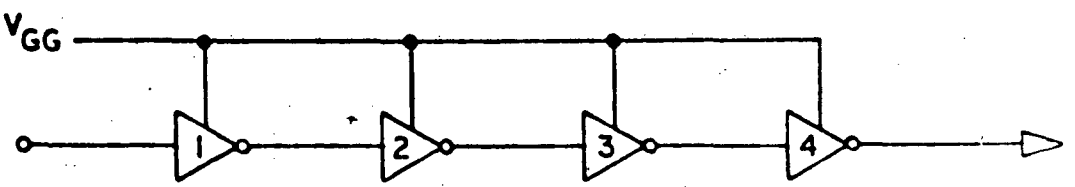

Fig. A-4. Typical four-delay inverter chain.

1. $V_{IN} = 0$

   $V_{OUT} = 0$

2. $V_{OUT} = V_{DD}$

3. $V_{OUT} = 0$

4. $V_{QUT} = V_{DD}$

For a completely internal device V_0 max is defined by

$$V_0 \text{ max} = V_T - V_N \tag{A-17}$$

where V_N is the allowable amount of system noise. Node 4 must discharge to V_0 max within the allowable number of time constants, assuming that all four inverters in the chain are fully loaded.

The allowable system noise voltage is then expressed in the following manner

Let V_{N1} be the logic-1 level of noise voltage

V_{N0} be the logic-0 level of noise voltage

Then $V_{IN2} = V_{OUT1} - V_{N1}$

$V_{IN3} = V_{OUT2} + V_{N0}$

$V_{IN4} = V_{OUT3} - V_{N1}$

The next step in the design procedure is to first choose a K_I/K_L ratio and then calculate the number of load-time constants required to reach V_0 max at node 4. V_I min is then defined as the value of V_{IN4} at the time when V_0 (4) reaches V_0 max.

The load and inverter-device sizes are then determined as follows:

$$R_{SC} = \frac{1}{K_L\left[2(V_{GG} - V_T) - V_{DD}\right]}$$

$$\frac{t}{\tau} = \frac{t}{R_{SC} C_L} = \frac{K_L \; t \left[2(V_{GG} - V_T) - V_{DD}\right]}{C_L}$$

Therefore,

$$K_L = \frac{\frac{(t)}{(\tau)} C_L}{\left[2 (V_{GG} - V_T) - V_{DD}\right] t} = K' \frac{W_L}{\ell_L}$$

and $$K_I = K' \frac{W_I}{\ell_I} = \frac{K_I}{K_L} K_L$$

Appendix B

LOGIC CIRCUIT DESIGN FOR MOS ARRAYS

A. RELATION BETWEEN INVERTER PARAMETERS

The basic inverter circuit is shown in Fig. B-1. Its requirements are to provide a logical One output where the input is a logical Zero and to provide a logical Zero output when the input is a logical One. Although power supply tolerances and environmental conditions result in variations in the One and Zero logic levels, the logic levels must not exceed certain limits if reliable operation is to be maintained. Thus, a logical One which corresponds to a high-output-voltage must not decrease below a certain minimum voltage, V_1 min, for which the circuit is designed. Similarly, a logical Zero which corresponds to a low output voltage must not increase above a certain maximum voltage, V_0 max. The required V_0 max is dictated by the threshold voltage, V_T, and the required Zero level noise immunity, V_{N0}.
Thus,

$$V_0 \text{ max} = V_T - V_{N0} \tag{B-1}$$

Since V_0 max is produced by the voltage divider action of the inverter and load devices, it is dependent on their conductance ratio. This conductance ratio is related to the geometry of the two devices as expressed by their K_I/K_L ratio, V_{DD}, V_{GG} and V_1 min. When a circuit is designed with a relatively large V_1 min, the inverter conductance for a given K_I increases thereby requiring a lower K_I/K_L ratio. On the other hand, a design with a relatively small V_1min requires a higher K_I/K_L ratio.

Other performance characteristics, such as device size, power dissipation and operating reliability, are also a function of the K_I/K_L ratio. Since small device size, low power dissipation and maximum reliability are the major goals of this design, a knowledge of these relationships is necessary in making an optimum choice. Figure B-2 shows how these parameters vary as a function of the K_I/K_L ratio. These results

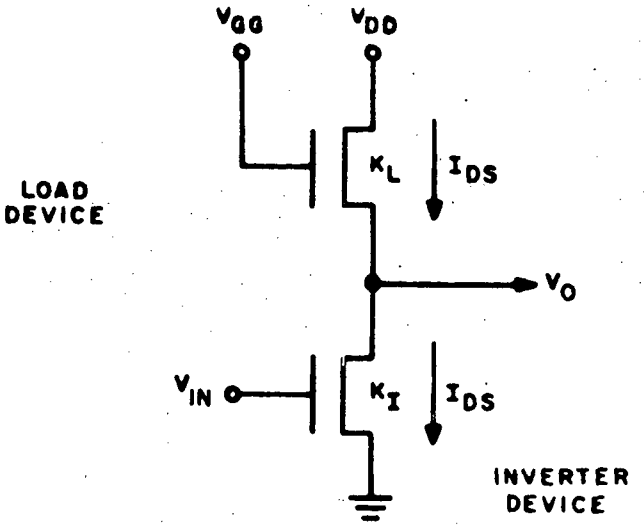

Fig. B-1. Basic MOS inverter circuit.

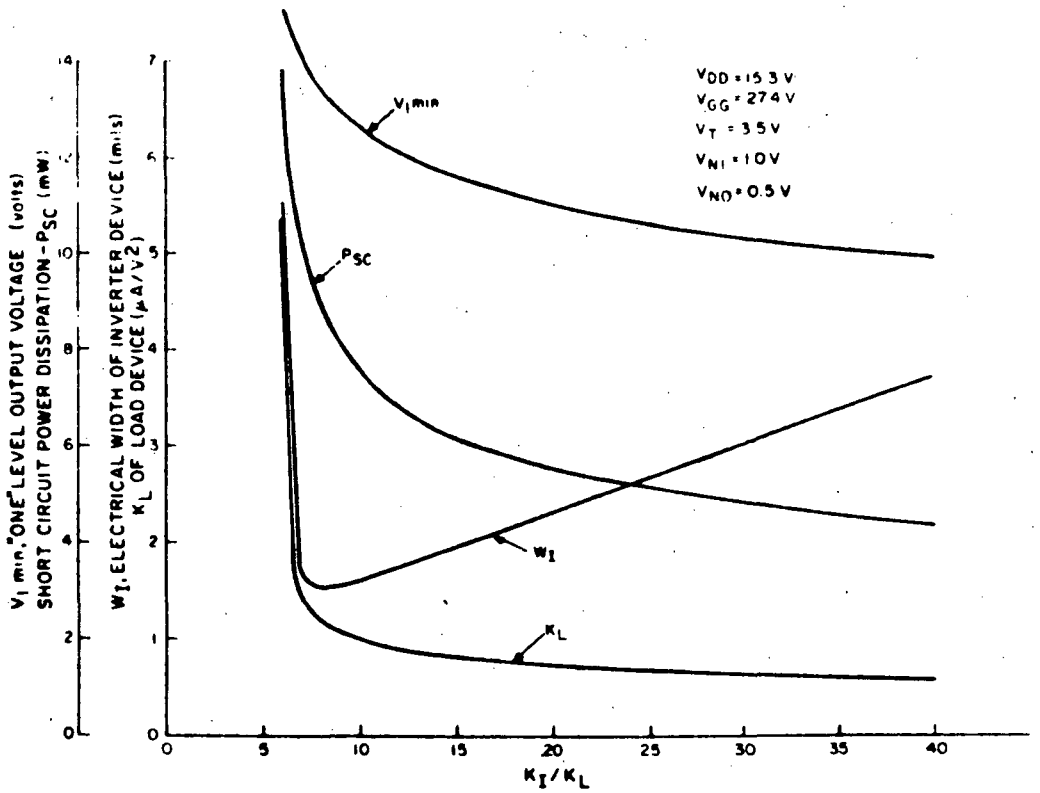

Fig. B-2. Relation between parameters of MOS inverter.

were obtained using the transient analysis program to compute these parameters for a chain of four inverters whose total progation delay under fully loaded conditions must not exceed 525 ns. The relationships of the parameters in Fig. B-2 may be understood by analyzing the basic inverter circuit of Fig. B-1. Here, the drain current I_{DS} may be expressed as

$$I_{DS} = K_L \left[2 (V_{GG} - V_0 - V_T) (V_{DD} - V_0) - (V_{DD} - V_0)^2 \right] \qquad \text{(B-1)}$$

Under static conditions, this drain current must be absorbed by the inverter device. Consequently, the drain current can also be expressed as

$$I_{DS} = K_I \left[2 (V_{IN} - V_T) V_0 - V_0^2 \right] \quad \text{for} \quad \left| V_{IN} - V_T \right| > V_0 \qquad \text{(B-2)}$$

$$I_{DS} = K_I \left[V_{IN} - V_T \right]^2 ; \quad \text{for} \quad \left| V_{IN} - V_T \right| < V_0 \qquad \text{(B-3)}$$

Combining equations (B-1) and (B-2) results in

$$K_I/K_L = \frac{2 (V_{GG} - V_0 - V_T) (V_{DD} - V_0) - (V_{DD} - V_0)^2}{2 (V_{IN} - V_T) V_0 - V_0^2} \qquad \text{(B-4)}$$

$$\text{for;} \quad \left| V_{IN} - V_T \right| > V_0$$

Combining equations (B-1) and (B-3) gives

$$K_I/K_L = \frac{2(V_{GG} - V_0 - V_T') (V_{DD} - V_0) - (V_{DD} - V_0)^2}{\left[V_{IN} - V_T \right]^2} \qquad \text{(B-5)}$$

$$\text{for} \quad \left| V_{IN} - V_T \right| < V_0$$

where $V_{IN} = V_1 \text{ min} - V_{N1}$ (One-level noise immunity). Equations (B-4) and (B-5) indicate that as the K_I/K_L ratio is increased, the required V_{IN} decreases. Since V $V_{IN} = V_1 \text{ min} - V_{N1}$, then V_1 min also decreases as the K_I/K_L ratio is increased.

This relationship is shown in Fig. B-2. Furthermore, since the maximum value of V_{IN} is limited by V_{DD}, there is a minimum K_I/K_L ratio below which Equations (B-4) and (B-5) cannot be satisfied. In Fig. B-1 this minimum K ratio is approximately 6. The general shape of the K_L curve can be understood by noting that K_L is directly proportional to the conductance of the load. In order to obtain a larger V_{IN} in the 525-ns time interval, the load conductance must be larger. Consequently, to obtain the maximum available V_{IN}, an infinite K_L is required. As the required V_1min is reduced, the required K_L decreases. With the aid of the K_L curve, the W_I curve can now be understood. Before proceeding to the W_I curve it should be noted that

$$W_I = (K_I/K') \ell_I \tag{B-6}$$

In order to keep device size to a minimum, the minimum allowable spacing is always used for the inverter length. Consequently W_I is directly proportional to K_I. The value of K_I can be written as a product of the K_I/K_L ratio and K_L so that

$$K_I = (K_I/K_L)(K_L) \tag{B-7}$$

If the above equation is evaluated with the data of Fig. B-2, it can be seen that in the region where K_I/K_L is small, the required K_L is very large, thereby requiring a large K_I to provide evan a low K_I/K_L ratio. It can also be seen from Fig. B-1 that a small increase in K_I/K_L ratio results in a large decrease in K_L, which according to equation (B-7) results in a large decrease in K_I. Consequently, W_I is large for low values of K_I/K_L and decreases rapidly as K_I/K_L is increased. For larger K_I/K_L ratios, K_L is much less sensitive to a change in K_I/K_L ratio. Thus, an increase in K_I/K_L results in a relatively small decrease in K_L. This produces a net increase in K_I and W_I. From here on, an almost linear relation exists between W_I and K_I/K_L. The curve of short circuit power dissipation has the same shape as the K_L curve, since the drain current (I_{DS}) is directly proportional to K_L and the short circuit power dissipation is $P_{SC} = I_{DS} \cdot V_{DD}$.

B. DESIGN COMPATIBILITY

A major requirement in this design is that the same set of masks be used for both the shallow and deep diffusion processes. As indicated in Table B-I, the two processes have different K's and different underdiffusions which cause a set of masks to have different electrical parameters in each of the processes. Since all devices on a chip are part of the same process, their performance parameters are the same. This makes all the gates on the same chip compatible with regard to logic levels and other characteristics. In order to achieve similar compatibility between chips of different processes, output buffers are always provided. One of the functions of these buffers is to provide an output logic level of sufficient magnitude to drive any chip regardless of its process and internal electrical characteristics. This still leaves the problem of assuring that a set of masks which may be an optimum selection for one process will be close to optimum or even function with the other process. Fortunately, as indicated in Fig. B-2, many designs are possible that permit the selection of a set of masks that operate with one K_I/K_L ratio for one process and with a different K_I/K_L ratio for another process. Different sets of masks can be tried and their resulting design parameters obtained. Finally, a set of masks is selected which has the smallest device sizes that still satisfy the performance requirements with both processes.

To facilitate evaluation and selection of possible designs, it is convenient to plot W_I instead of K_I. The relation between the two is

$$W_I = K_I/K' \left[L_I - 2 U_D \right] \tag{B-8}$$

where

W_I = the electrical width of the inverter device

L_I = the mask length of the inverter device

U_D = the underdiffusion.

Since K', L_I and U_D are constants, W_I has the same shape as K_I. However, a given value of K_I results in different values of W_I in the two processes. This is due to the different values of K' and U_D in the two processes. In order to keep device size as small as possible, the minimum permissible $L_I = .4$ mil is always used for mask length of the inverter device. The value of K' used is the minimum that can result with a given process. This includes K' reductions due to process tolerances and reductions due to the upper temperature limit of +135°C. The minimum K' is used since according to equation (B-8) this results in the largest W_I requirement. Thus, for example for $K_I = 20 \times 10^{-6}$, the resulting W_I becomes

$$W_I = \frac{20 \times 10^{-6}}{1.86 \times 10^{-6}} \left[.4 - 2\,(.05)\right] = 3.23 \text{ mils for the shallow diffusion process}$$

and

$$W_I = \frac{20 \times 10^{-6}}{1.12 \times 10^{-6}} \left[.4 - 2\,(.12)\right] = 2.86 \text{ mils for the deep diffusion process}$$

In this manner a W_I curve may be obtained for each process.

Before plotting these curves another worst-case consideration must be introduced. The curves of Fig. B-2 have been obtained for one set of voltages namely V_{DD} max = 15.3, V_{GG} max = 27.4, and V_T min = 3.5. Undoubtedly, different sets of curves are obtained when each of these voltages goes to its other extreme. Eight combinations are possible. However, the power supply system is designed so that V_{DD} and V_{GG} always track so that the condition of V_{DD} max and V_{GG} min or V_{DD} min and V_{GG} max do not occur. This reduces to four the number of possible combinations. Data was obtained for all four combinations which indicated that below a $K_I/K_L = 6.5$, V_{DD} max, V_{GG} max and V_T min present a worst case for minimum W_I requirements, whereas above a $K_I/K_L = 6.5$, V_{DD} min, V_{GG} min and V_T max present a worst-case for the minimum W_I requirement. The other two sets of voltages do not present worst-case requirements. The design curves are therefore composites of the worst-case W_I curve prevailing in a given K_I/K_L region. A set of these curves for the 4-pF family is shown in Fig. B-3, Fig. B-4 and Fig. B-5. In this procedure the W_I curves are constructed first, using the largest values of W_I. Construction of the curves of Fig. B-3 is then accomplished by using the K_L and P_{SC} which correspond to the selected value of W_I.

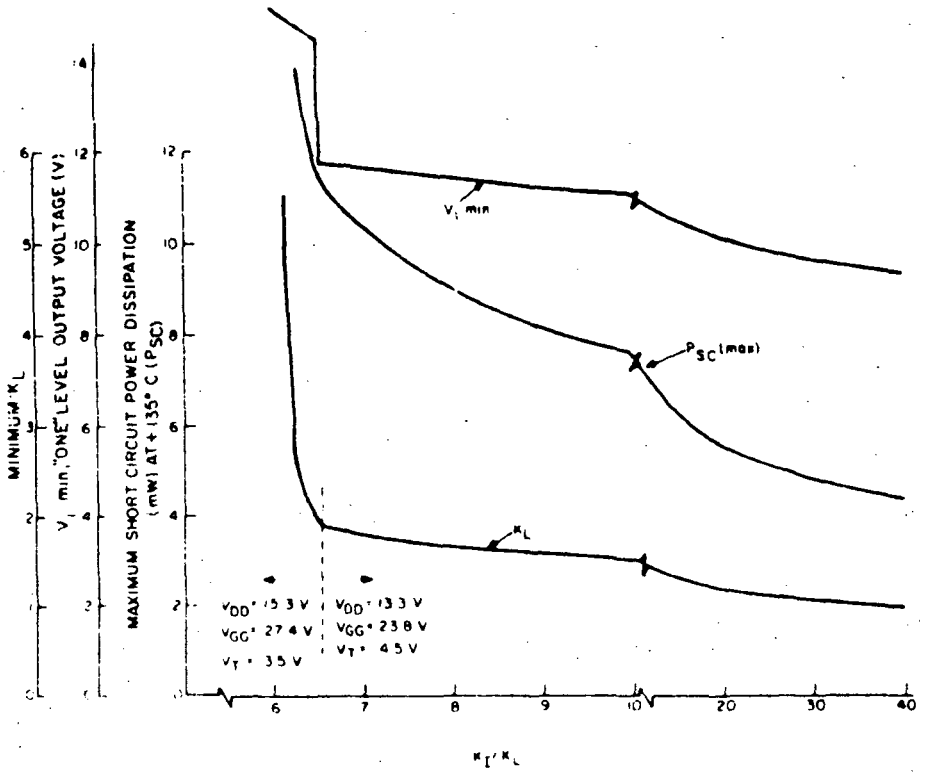

Fig. B-3. Short-circuit power dissipation and minimum K_L vs. K_I/K_L.

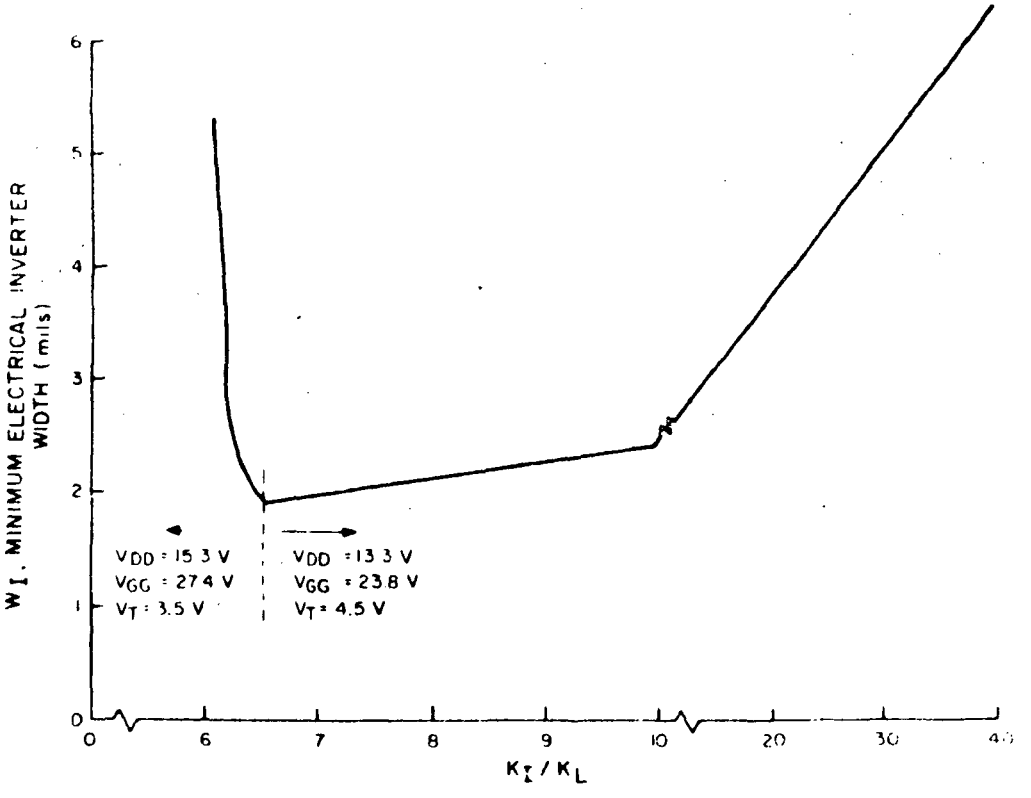

Fig. B-4. Inverter width vs. K_I/K_L for the shallow diffusion process.

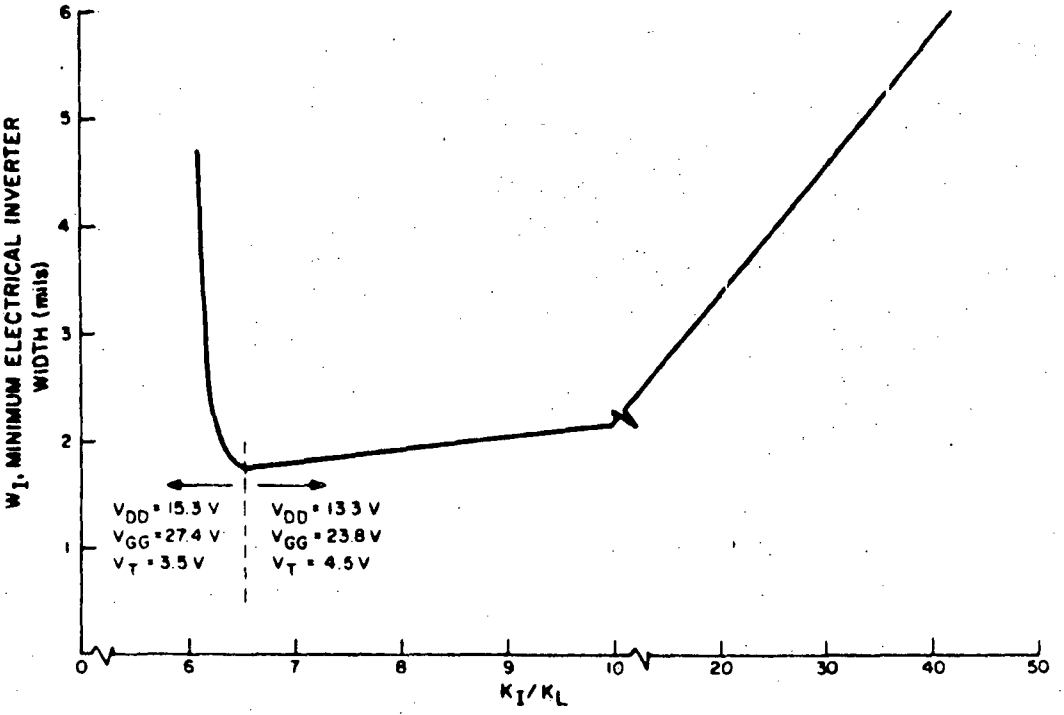

Fig. B-5. Inverter width vs. K_I/K_L for the deep diffusion process.

C. DESIGN PROCEDURE FOR INVERTER

Although the curves show a continuous relation between circuit parameters and K_I/K_L, practical considerations permit design only at discrete points. For example, minimum width and spacing restriction allow all devices to be drawn to the nearest 1/10 mil. Thus the minimum load size can have dimensions of $W_L = .3$ and $L_L = .6$. The next larger size is $W_L = .4$, $L_L = .6$ or $W_L = .3$, $L_L = .7$ etc. Since there are only about 10 to 20 W_L and L_L combinations which result in acceptable size and K_L, it is convenient to start the design by assuming some load dimension for which all performance parameters can be calculated from the curves.

A systematic procedure for doing this is to start with the minimum size load transistor which minimum width and spacing restrictions will allow. This is found

to be

$$W_L = .3 \text{ mil} \quad L_L = .6 \text{ mil}$$

the corresponding K_L value can now be calculated as

$$K_L = K' \frac{W_L}{L_L - 2\,U_D} = 1.86 \times 10^{-6} \quad \frac{.3}{.6 - 2\,(.05)} = 1.1 \times 10^{-6} \qquad \text{(B-8)}$$

for the shallow diffusion process. As explained earlier a different value of K_L will result for the deep diffusion process. A complete design will be carried out first for the shallow and then for the deep diffusion process. Using the K_L value of 1.1×10^{-6}, Fig. B-3 yields, a $K_I/K_L = 24$ and a V_1 min = 9.9 V. Using the obtained K_I/K_L ratio, Fig. B-4 yields a required $W_I = 4.3$. Figure B-3 also provides the corresponding power dissipation.

Using the same mask size, the comparable K_L is

$$K_L = K' \frac{W_L}{L_L - 2\,UD} = 1.12 \times 10^{-6} \quad \frac{.3}{.6 - 2\,(.12)} = .93 \times 10^{-6}$$

for the deep diffusion process. For a $K_L = .93 \times 10.6$, Fig. B-3 yields a required $K_I/K_L > 40$ and $V_{1M} < 9.3$ V. Using the obtained K_I/K_L ratio Fig. B-4 yields a required $W_I > 6$ mils. This computation is repeated for other loads for which either W_L or L_L is incremented by 1/10 mil. These results are tabulated in Table B-1. Some of the design trials such as No. 1, No. 6, and No. 7 require relatively large inverter W_I which would result in proportionally large area. Consequently, they are eliminated from further consideration. Also design trials with $W_L > .7$ with $L_L = .6$ are eliminated since a point of excessive power dissipation is being reached. Design trials are also terminated for $W_L > .7$ with $L_L = .7$ since the area taken by the load device starts exceeding the desirable limit and consequently imposes severe restriction on cell layout. Thus the choice is narrowed down to trials No. 2, 3, 4, 5, 8, 9, 10. From these trial designs, the remaiming possible designs of interest are

tabulated on the right side of Table B-I. At this point it is appropriate to introduce a requirement that the deep diffusion process K ratio = $K_I/K_L \geq 12$ which resulted from a study of the Zero level noise conditions and transient behavior. This is due to worst case considerations of transferring a logical Zero from one phase to the next. Due to gate to drain (Miller) capacity, the inverted Zero input is fed back to the input gate causing the inverter to partially conduct. This in turn results in a reduction of the logical One output. The minimum K_I/K_L requirement is to assure reliable operation for this worst case condition. This requirement can be met either by selecting those designs where with the deep diffusion process the $K_I/K_L \geq 12$ (design trials 2, 8) or by increasing the W_I. For design trial No. 2, the $K_I/K_L > 12$ and the required mask $W_I = 2.9$ mils. In the inverter the mask W_I is smaller than the electrical W_I due to the underdiffusion. This is the smallest value of W_I which will satisfy the deep diffusion process requirements. Even though a smaller W_I could be used in the shallow diffusion process, its mask W_I must be the same for both processes. This results in an over-design for the shallow diffusion process. The increase in W_I results in a change of the design parameters. The recalculated values are tabulated under the heading of acceptable designs. The actual K_I/K_L is calculated from

$$K_I/K_L = \frac{K' \dfrac{W_I + U_D}{L_I - 2U_D}}{K' \dfrac{W_L}{L_L - 2U_d}} = \frac{\dfrac{2.9 + .05}{.4 - 2(.05)}}{\dfrac{.4}{.6 - 2(.05)}} = 12.3 \qquad \text{(B-9)}$$

for the shallow diffusion process. Equation (B-9) may require some explanation. When calculating the electrical width of the inverter resulting from its mask width, the underdiffusion due to only one side is added. This is due to consideration of layout rules and misalignment between the gate oxide and the source or drain p-regions. When calculating the electrical width of the load, no underdiffusion is added to the mask W_L. This is due to the manner in which the load device is constructed; this is evident from the layout rules.

TABLE B-I POSSIBLE INVERTER DESIGNS FOR 4-pF FAMILY

DESIGN NO.	LOAD MASK SIZE		SHALLOW DIFFUSION PARAMETERS					DEEP DIFFUSION PARAMETERS					ACCEPTABLE DESIGNS						
														SHALLOW			DEEP		
	W_L	L_L	K_L	W_I	$\frac{K_I}{K_L}$	PSC	VIM	K_L	W_I	$\frac{K_I}{K_L}$	PSC	VIM	W_I	$\frac{K_I}{K_L}$	PSC	VIM	$\frac{K_I}{K_L}$	PSC	VIM
1	.3	.6	1.1	4.3	24		9.9	.93	6	>40		<9.3	-	-	-	-	-	-	-
2	.4	.6	1.5	2.5	10		11.1	1.24	3.0	17		10.3	2.9	12.3	7.6	10.8	17	5.9	10.3
3	.5	.6	1.86	1.9	6.5		11.8	1.55	2.1	9.3		11.2	2.6	8.9	11.4	11.3	12	8.0	10.9
4	.6	.6	2.2	2.2	6.35		14.7	1.86	1.8	6.5		11.8	3.2	9.0	12.6	11.3	12	11.4	10.9
5	.7	.6	2.6	2.6	6.23		14.9	2.17	1.9	6.38		14.3	3.6	8.7	14.0	11.3	12	12.4	10.9
6	.3	.7	.93	6.3	10		<9.3	.73	>6	>40		<9.3	-	-	-	-	-	-	-
7	.4	.7	1.24	3.4	17		10.3	.97	5.8	40		9.3	-	-	-	-	-	-	-
8	.5	.7	1.55	2.3	9.3		11.2	1.2	3.2	18.5		10.2	3.4	12.6	6.9	10.7	18.5	5.7	10.2
9	.6	.7	1.86	1.9	6.5		11.8	1.46	2.3	11		11.0	2.4	8.2	11.4	11.4	12	7.2	10.9
10	.7	.7	2.17	2.2	6.38		14.3	1.7	1.9	7.6		11.5	2.9	8.4	12.4	11.1	12	9.5	10.9
11	.8	.7																	

It is important to distinguish between the meaning of V_1 min's in Table B-I. The first tabulation lists the available V_1 min which is determined by the available K_L. The second tabulation is the required V_1 min which is equal to or smaller than that available. This is due to the fact that W_I and K_I/K_L have been increased.

Attention is now turned to design trial No. 3 whose deep diffusion process $K_I/K_L < 12$. Here the K_I/K_L is increased by increasing W_I. This requires a recalculation of resulting parameters for both processes as was done with Design No. 2. This procedure is continued for all trial designs of interest. A design choice is now made, based on a compromise between minimum W_I, minimum power dissipation, and minimum dimensions for load device. Based on these considerations, Design No. 3 was selected as the best compromise to meet the requirements. The effects of stray circuit resistance required further modification of the design. The final mask dimensions used are tabulated on page B-27 .

D. DESIGN OF 2-pF FAMILY

The design procedure for the 2-pF family is essentially the same as that for the 4-pF family. The graphs of Fig. B-3 to Fig. B-5 can also be used for designing the 2-pF family if the ordinates are divided by a factor of two. Table B-II is made up and from it a design is selected. It must be noted, however, that since the 4-pF family is already designed, it restricts the design choice for the 2-pF family. This is due to the fact that the 4-pF and 2-pF families of the same process must be compatible. This means that the output levels (V_1 min, V_0 max) of the 2-pF family must be sufficient to satisfy the requirements of the 4-pF family and vice versa. This requirement is satisfied by first selecting a design where the 2-pF available V_1 min of the 4-pF family is equal to or greater than the required V_1 min of the 2-pF family, W_I of the chosen 2-pF family is increased if necessary. Based on these considerations, Design No. 9 of Table B-II was selected for the 2-pF family.

TABLE B-II POSSIBLE INVERTER DESIGNS FOR 2-pF FAMILY

DESIGN NO.	LOAD MASK SIZE		SHALLOW DIFFUSION PARAMETERS					DEEP DIFFUSION PARAMETERS					ACCEPTABLE DESIGNS						
														SHALLOW			DEEP		
	W_L	L_L	K_L	W_I	$\frac{K_I}{K_L}$	PSC	VIM	K_L	W_I	$\frac{K_I}{K_L}$	PSC	VIM	W_I	$\frac{K_I}{K_L}$	PSC	VIM	$\frac{K_I}{K_L}$	PSC	VIM
1	.3	.6	1.1	1.1	6.35		14.7	.93	.9	6.5		11.8	1.6	9.5	12.6	11.2	12	12.0	10.8
2	.4	.6	1.5	1.5	6.19		14.9	1.24	1.1	6.26		14.8	2.0	8.4	15.0	11.4	12	14.0	10.8
3	.5	.6	1.86	2.0	6.15		15.0	1.55	1.4	6.18		14.9	-	-	-	-	-	-	-
4	.3	.7	.93	.98	6.5		11.8	.73	1.1	10.5		11.1	1.2	8.3	11.4	11.4	12	7.5	10.8
5	.4	.7	1.24	1.25	6.25		14.8	.97	.9	6.48		11.8	1.6	8.3	14.0	11.4	12	9.5	10.8
6	.5	.7	1.55	1.6	6.18		14.9	1.2	1.1	6.29		14.8	2.0	7.9	15.0	11.5	12	13.4	10.8
7	.6	.7	1.86	2.0	6.15		15.0	1.48	1.4	6.19		14.9	-	-	-	-	-	-	-
8	.3	.8	.8	1.1	8.5		8.5	.6	1.6	18		10.3	1.5	11.9	8.5	10.9	18	5.8	10.3
9	.4	.8	1.06	1.05	6.4		11.8	.8	1.0	8.5		11.3	1.3	8.2	12.0	11.4	12	8.5	10.8

E. DESIGN OF INVERTER WITH COUPLING DEVICE

Another basic logic block is the inverter with a coupling gate. The circuit for this configuration is shown in Fig. B-6a. This gate can be used as unit logic delay or to prevent the transmission of information. This logic element must be compatible with the basic inverter in such a way that when it replaces an inverter in a chain of 4, the total delay of the chain must not increase. Possible locations of an inverter with transmission gates in a 4-stage chain are illustrated in Fig. B-6b. In each case the delay from A to B must not exceed the delay of the upper most chain. The design of this logic element is complicated by the fact that a choice of any one of the transistors affects the choice of the other two. Therefore, many combinations must be evaluated in order to find an optimum design. It is uneconomical to make exact evaluation of each combination. Consequently, the transient analysis program was used to provide an approximate but reasonably accurate analysis of many device combinations without using excessive computer time. The selected design was then thoroughly evaluated.

The model used in the first order analysis is shown in Fig. B-7. Here the previously designed 4-pF inverters (3, 4, 5, 7) are used as a basis for propagation delay comparison. Gates 1, 2 are used to simulate the condition when the output of an inverter with a transmission device are switched to V_1 min and Gate 6 simulates the conditions when its output switches to V_0 max. An assumed device combination is acceptable if the following two conditions are satisfied.

(1) The delay of stages 1 and 2 $\leq$ delay of stages 3 and 4.

(2) The delay of stage 6 $\leq$ delay of stage 7.

The relation between the parameters corresponding to acceptable desins are shown in Fig. B-8. It can be seen that for relatively small values of W_C, the required W_{IC}, K_{LC} and P_{SC} are relatively high and that they decrease rapidiy for increasing W_C. When W_C is increased from .5 mil to .9, the required W_{IC} decreases from 6.7 to 4.2 mil. Consequently for efficient area utilization it is desirable to operate with a relatively large W_C. The upper limit on W_C is determined by noise and layout considerations. An excessively large W_C could deteriorate the "one" level (V_1 min)

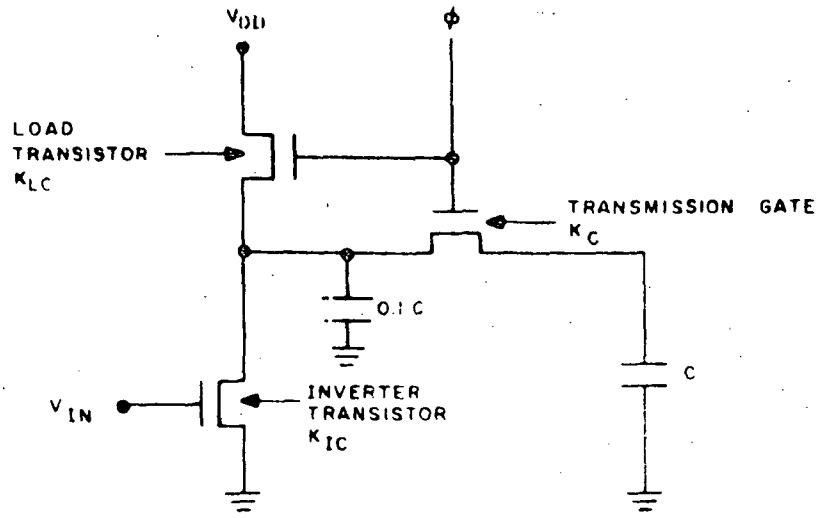

Fig. B-6a. Inverter with transmission gate.

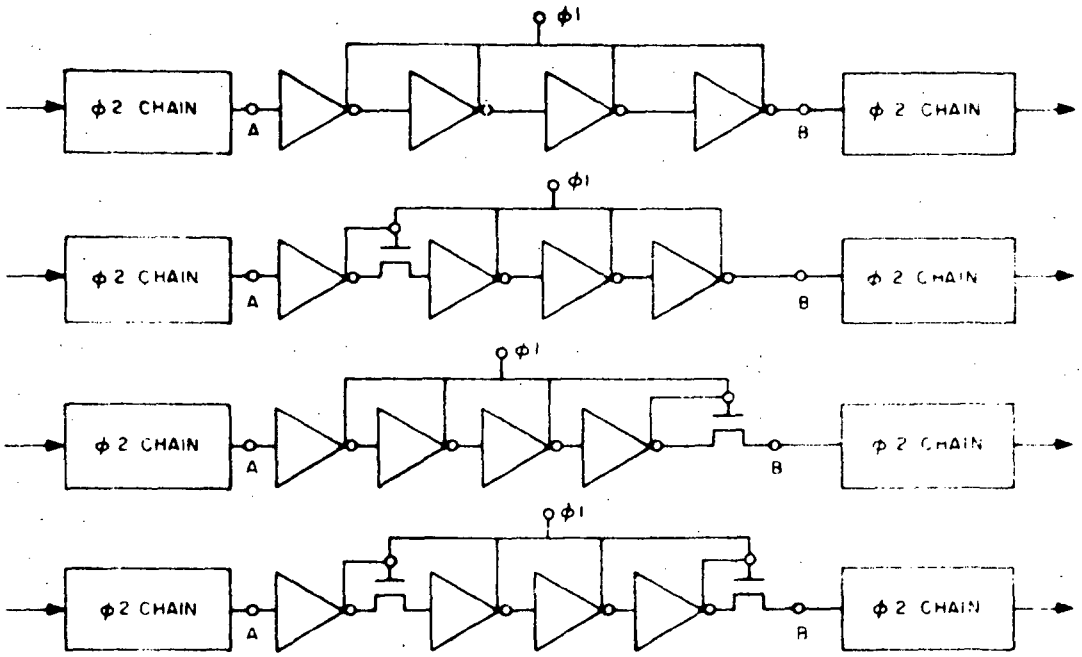

Fig. B-6b. Possible locations of inverter with transmission gate.

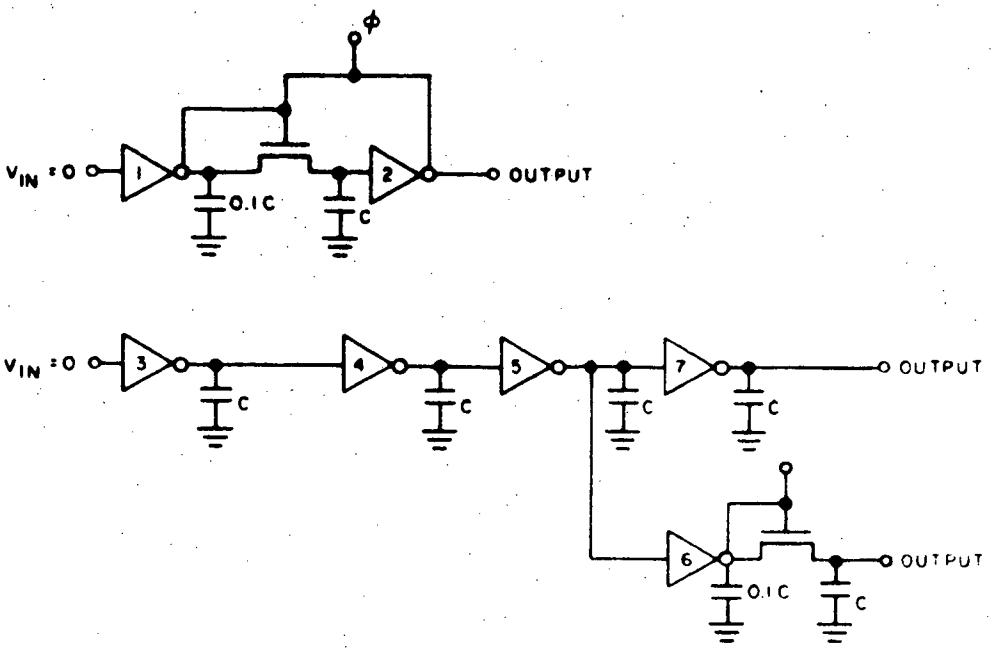

Fig. B-7. Logic chains used to design inverter with transmission gate.

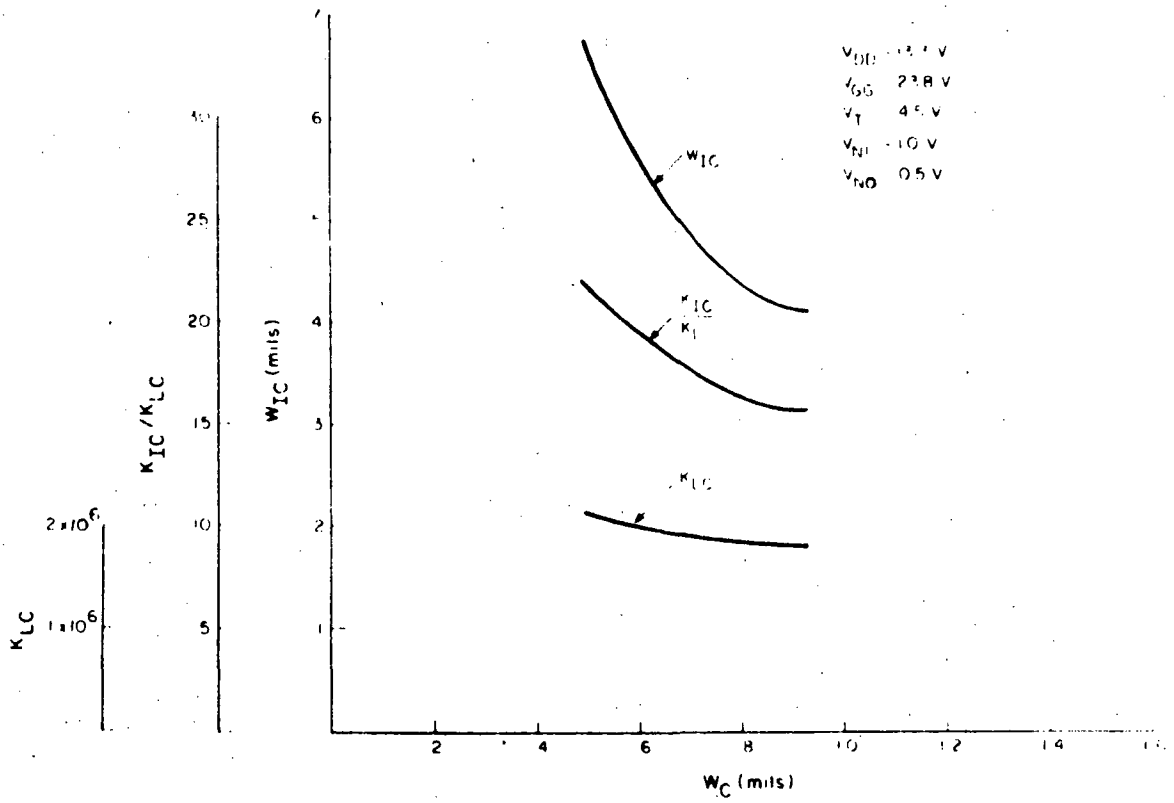

Fig. B-8. Relationship between parameters of inverter with transmission device.

during positive transition of the clock phase and may not be compatible with the existing power bus structure. The layout considerations indicated that a W_C up to 1.5 mil would present no problems.

In order to make a final selection of devices and to guarantee that worst case dynamic and static conditions are satisfied, a more detailed analysis was carried out. This analysis included all significant stray capacities, "body effect" and "early effect". In addition realistic clock waveforms were used. Various worst case conditions were discovered and device sizes were altered slightly so as to satisfy worst case requirements. The circuit used for this study consisted of a chain of four inverters driving another chain of four inverters via a transmission gate. With this model various worst case conditions were simulated for transferring a logical One and a logical Zero using device sizes and process constants for each process. In addition, analysis with and without "early effect" were compared, resulting in the conclusion that the worst case results when "early effect" is not included. Subsequent evaluations were therefore made without early effect. This procedure resulted in the selection of device sizes having the following values for 4-pF family.

W_{LC}	= 0.6 mil	L_{LC}	= 0.6 mil
W_{IC}	= 4.2 mils	L_{IC}	= 0.4 mil
W_C	= 1.0 mil	L_C	= 0.4 mil

The device sizes for the 2-pF family are

W_{LC}	= 0.3 mil	L_{LC}	= 0.6 mil
W_{IC}	= 2.1 mils	L_{IC}	= 0.4 mil
W_C	= 0.5 mil	L_C	= 0.4 mil

F. STRAY RESISTANCE CONSIDERATIONS

Up to now the effects of stray resistances in MOS circuits were not included in the design. Such resistances exist primarily as a result of interconnections made by p regions. Figure B-9 shows a typical layout with its associated resistances. The resistance is measured in squares and multiplied by the resistivity per square which

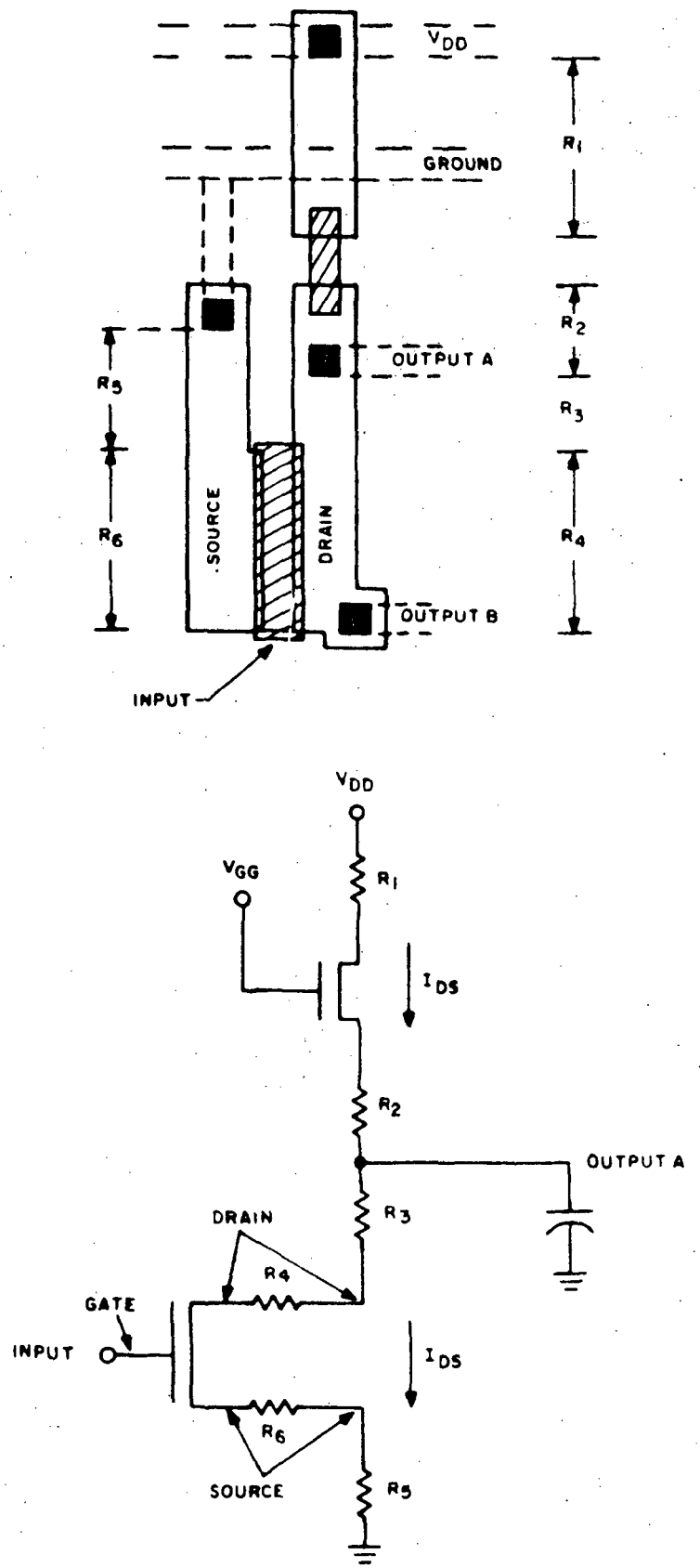

Fig. B-9. Stray resistance in MOS circuit.

ranges from 100-150Ωfor the two processes involved. Generally stray resistance has a detrimental effect on performance and should be kept to a minimum. The degree to which it effects performance depends on its location. The effect of resistors R_1 and R_2 is to increase the charging time and thereby cause a reduction in speed. The effects of R_3, R_4, R_5 and R_6 are more serious since they deteriorate the Zero level which could prevent operation at any speed. The deterioration of the Zero level becomes more severe as K' increases. This is due to the fact that the resistance of the load device and that of the inverter decrease as K' increases. With zero stray resistance, this has no effect on the Zero level output voltage, since the ratio of inverter to load resistance remains constant. However, when stray resistances R_3 and R_6 are present, this resistance ratio is increased, thereby increasing the magnitude of V_0 max. The extent of damage produced by resistors R_3 through R_6 is a function of their location. For example, R_3 increases V_0 max by an amount $I_{DS}R_3$ where I_{DS} is the drain current. Resistance R_4 which is located in the active drain region does not conduct the full current I_{DS} since parts of it are shunted away by the inverter device which is conducting. Consequently, the voltage drop across R_4 is proportionally less than that across R_3. Similar reasoning can be applied to R_6 as was applied to R_4, however R_6 in addition to increasing the V_0 max due to its own voltage drop also increases the voltage drop of the inverter device by reducing the gate to source voltage. Most damaging of all is resistor R_5 which increases V_0 max by its $I_{DS}R_5$ drop and also reduces the gate to source voltage by the same amount. The relative effects of resistors R_3 to R_6 were evaluated with the circuit model of Fig. B-10. To do this, the inverter device is sliced into n sections. The width of each section is made sufficiently small so that its distributed resistance can be approximated by a lumped resistor. Calculations are made with different values of stray resistances. In each case the inverter size required to absorb the same current and provide the same V_0 max is calculated. The results indicated that as each of the stray resistances is increased, the inverter device width has to be increased in order to maintain the same value of V_0 max. Furthermore, the circuit of Fig. 3-10 may be approximated by a simplified equivalent circuit if the stray resistances assume

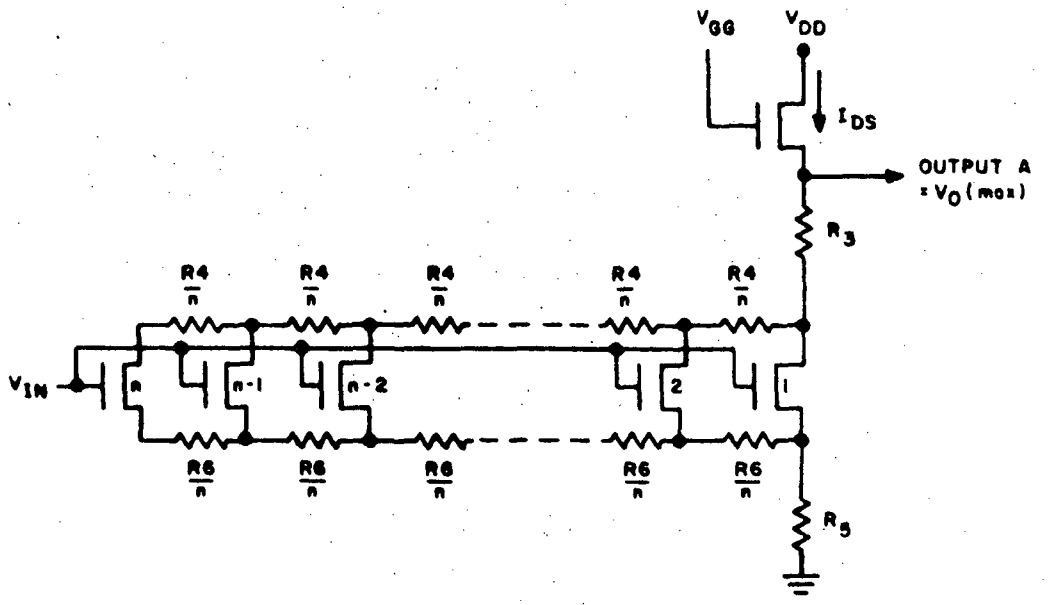

Fig. B-10. Model for calculating effective stray resistance.

weighting factors as shown in Fig. B-11. Thus, by attaching weighting factors to the individual resistors an equivalent stray resistance of the inverter device (R_{SI}) can be caluculated.

$$R_{SI} = R_3 + 0.25R_4 + 0.5R_6 + 2R_5 \tag{B-9}$$

Based on this analysis, an approximate expression is written for the equivalent stray resistance of the load device as

$$R_{SL} = R_1 + 1.5\,R_2 \tag{B-10}$$

The value of R_{SI} that can be tolerated depends on the upper limit of K', the K_I of the inverter device, and the amount by which the inverter K_I is increased over that required when the stray resistance is zero.

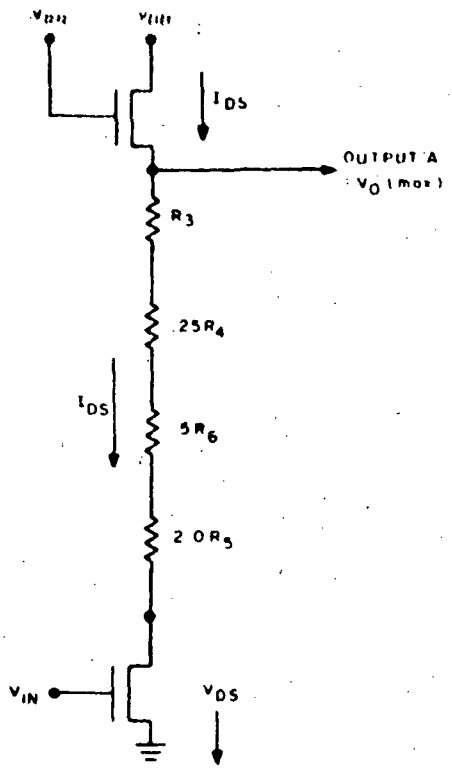

Fig. B-11. Simplified equivalent circuit of Fig. B-9.

The equivalent circuit of Fig. B-11 can be used to calculate the permissible stray resistance. Since the K_L of the load device and the required V_0 max are known, the drain current (I_{DS}) can be calculated as

$$I_{DS} = K' \frac{W_L}{L_L - 2U_d} \left[2(V_{GG} - V_T - V_0 \text{ max})(V_{DD} - V_0 \text{ max}) - (V_{DD} - V_0 \text{ max})^2\right] \quad \text{(B-11)}$$

The drain to source voltage (V_{DS}) of the inverter becomes

$$V_{DS} = V_0 \text{ max} - I_{DS} R_{SI} \quad \text{(B-12)}$$

and

$$K_I = \frac{I_{DS}}{2(V_{IN} - V_T) V_{DS} - V_{DS}^2} \quad \text{for} \quad |V_{IN} - V_T| > V_{DS} \tag{B-13}$$

$$K_I = \frac{I_{DS}}{(V_{IN} - V_T)^2} \quad \text{for} \quad |V_{IN} - V_T| < V_{DS} \tag{B-14}$$

as K' increases due variations in process or temperature, I_{DS} increases proportionally. This results in a decrease of V_{DS}. An increase in K' also results in faster operation, thereby increasing the value of V_{IN}. A reduction in V_{DS} tends to increase the required K_I while an increase in V_{IN} tends to decrease the required K_I. The values of R_{SI} and K' determine which of the two effects dominate. For extremely low values of R_{SI}, the required K_I decreases whereas for relatively large values of R_{SI}, the required K_I increases. Figure B-12 to Fig. B-15 show the relation between the K_I/K_L as a function of K' for values of R_{SI} = 0, 500 Ω and 1000 Ω. These curves are plotted for different sets of V_{DD}, V_{GG} and V_T voltages. It can be seen that for R_{SI} = 0, K_I/K_L decreases as K' is increased, which indicates that for R_{SI} = 0 the design for minimum K' represents a worst case. For R_{SI} = 500 Ω, the required K_I/K_L at minimum K' is about 10% larger; as K' increases, the required K_I/K_L remains relatively constant over a wide range of K'. For R_{SI} = 1000 Ω, the reduction in V_{DS} definitely dominates and the required K_I/K_L increases very rapidly for higher values of K'. From these results it can be concluded that in order to operate with high K', the resistance R_{SI} should not exceed 500 Ω. Since some resistance must be allowed in order to conserve chip area, the penalty paid for allowing 500 Ω is not too severe and results in a required 10% increase of the K_I of the inverter. These results were obtained for an inverter device width of 3 mils. They can be generalized to be applicable to any inverter width. Thus the allowable R_{SI} for an inverter of width W_I can be approximated as

$$R_{SI} = \frac{1500}{W_I} \ \Omega \tag{B-15}$$

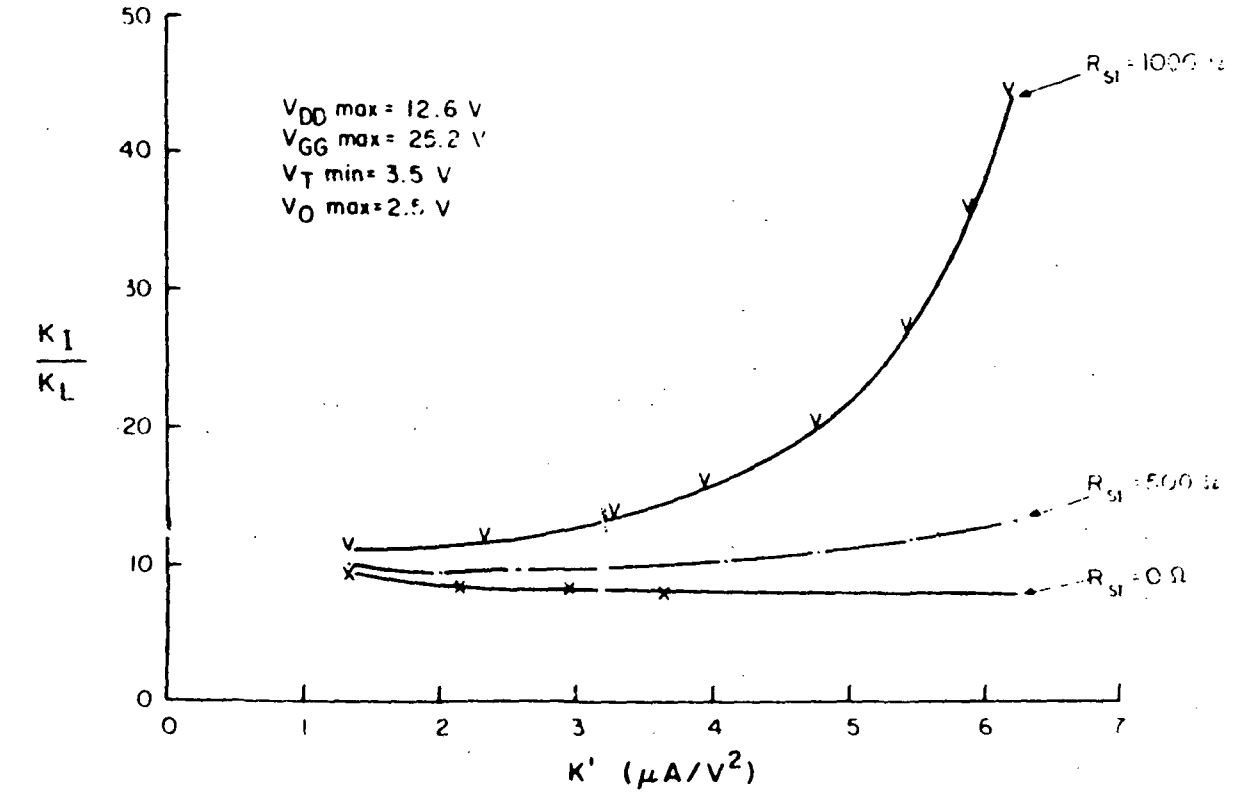

Fig. B-12. Effect of stray resistance on K_I/K_L.

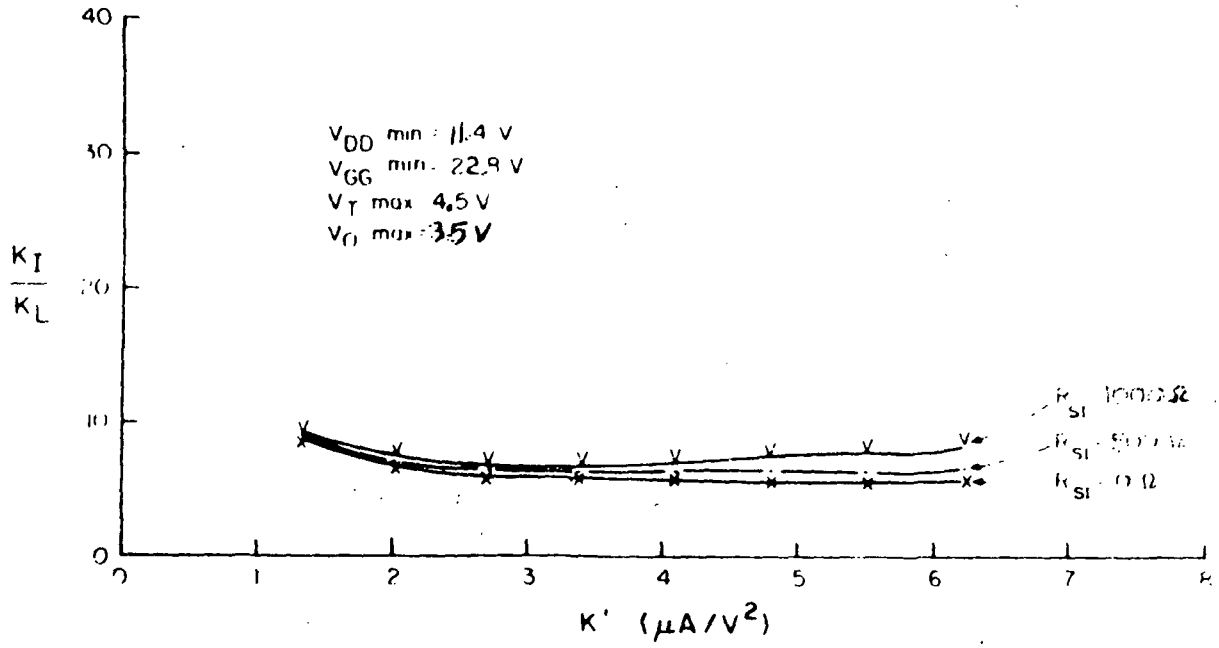

Fig. B-13. Effect of stray resistance on K_I/K_L.

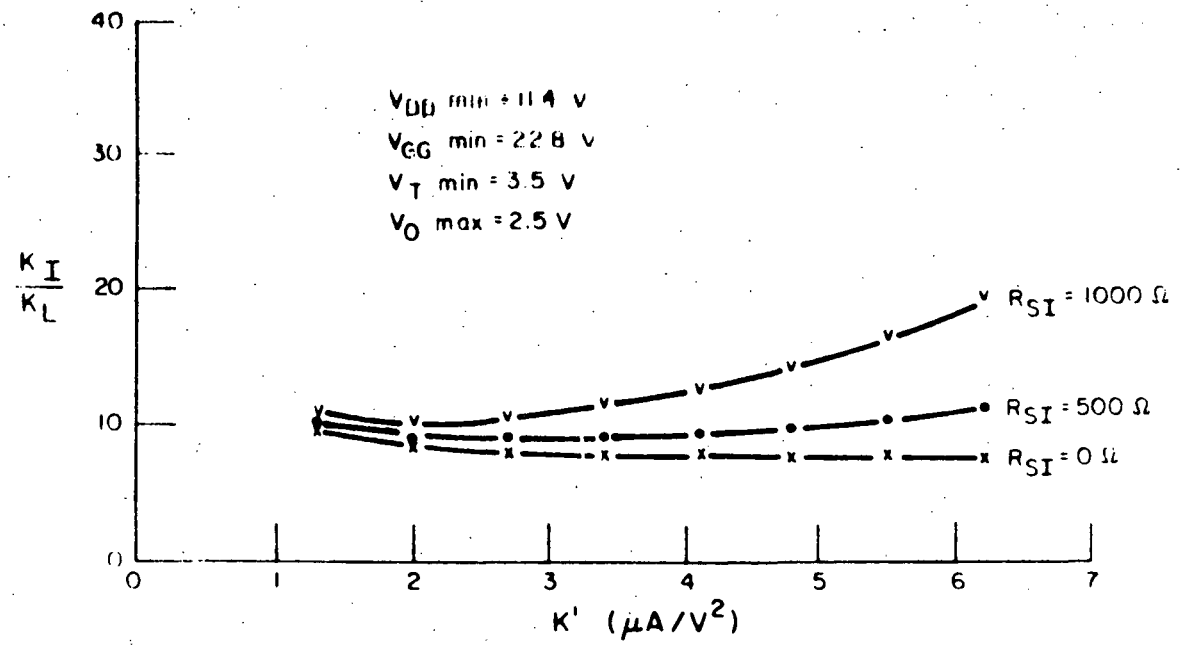

Fig. B-14. Effect of stray resistance on K_I/K_L.

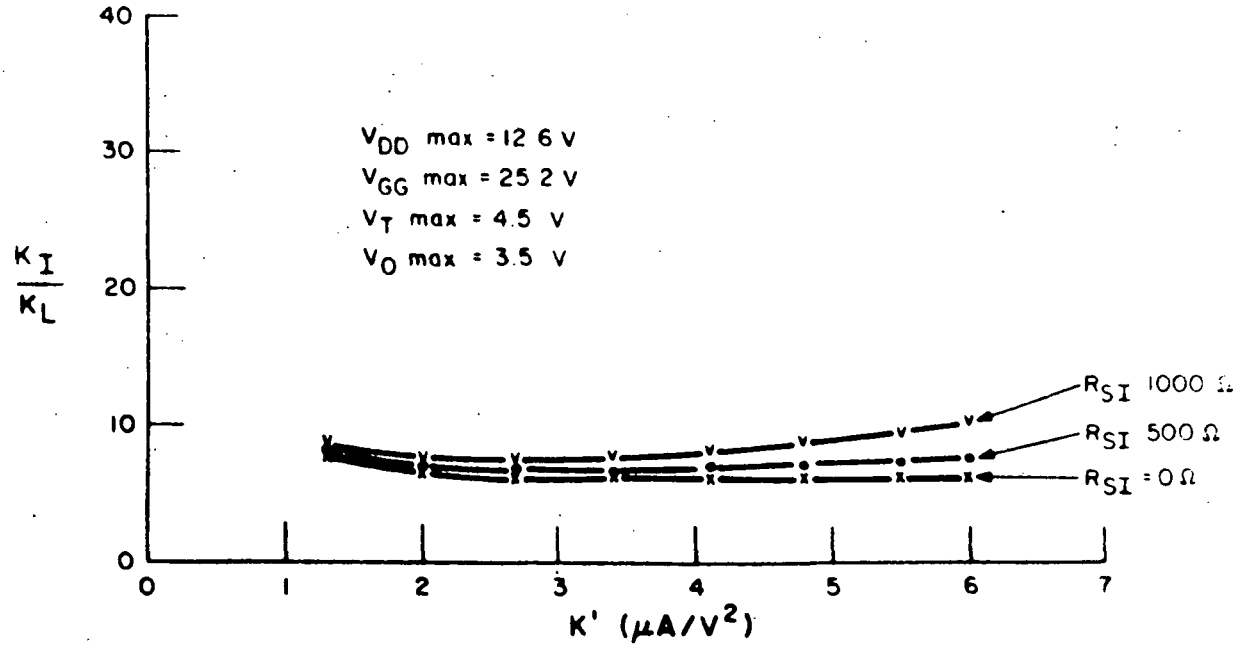

Fig. B-15. Effect of stray resistance on K_I/K_L.

B-24

where W_I is the mask width which includes a 10% increase for stray resistance compensation. This computation assumes an inverter device mask length of 0.4 mil and the process constants given in Table B-III. The results of equation B-9 and equation B-15 may be combined to provide a formula for calculating permissible stray resistance for an inverter device W_I. Thus

$$R_{SI} = R_3 + 0.25\,R_4 + 0.5\,R_6 + 2.0\,R_5 \leq \frac{1500}{W_I} \qquad \text{(B-16)}$$

It will be noted that the curves of Fig. B-12 to Fig. B-15 were obtained for V_{DD} and V_{GG} values which are somewhat different than the design voltages used here. Also, the Zero noise voltage V_{N0} = 1 volt thereby resulting in a V_0 max as low as 2.5 volts. This imposes more stringent requirements on stray resistance than the $|V_0 \text{ max}|$ = 3.0 volts in this design. The results may be somewhat pessimistic, a fact which was taken into account in deriving the stray resistance relationships. The load resistance R_{SL} and coupling device series resistance R_C for any member of the cell family must satisfy the following equations

$$R_{SL} = R_1 + 1.5\,R_2 \leq \frac{3 \times 10^{-3}}{K_L}$$

$$R_C = R_7 \leq \frac{6 \times 10^{-3}}{K_C} \qquad \text{(B-17)}$$

where R_7 is the total stray resistance in series with the coupling device. For equation B-17 the values of K at + 135°C should be used. The allowed value of stray resistance in the load can result in an approximate 2% increase in charge time. This is permitted on the basis that the required V_1 min is generally somewhat lower than the available V_1 min. A 5% increase in resistance is permissible in the coupling device since it has sufficient over-design. The amount of stray resistance present in the inverter device is a function of the layout and the point from which the output is taken. For example, stray resistances R_2, R_3, and R_4 can be prevented from affecting V_0 max by taking the output B in place of A in Fig. B-9. Under these conditions the only resistance that must be

considered is R_5 and R_6. The final mask dimensions which take into account stray resistance are listed below.

Inverter		
Load	4 pF	2 pF
Mask W_L	.5 mil	.4 mil
Mask L_L	.6 mil	.8 mil
Mask W_I	3.0 mils	1.5 mils
Mask L_I	.4 mil	.4 mil

Inverter with transmission device		
Load	4 pF	2 pF
Mask W_L	.6 mil	.3 mil
Mask L_L	.6 mil	.6 mil
Mask W_I	4.5 mils	2.3 mils
Mask L_I	.4 mil	.4 mil
Mask W_C	1.0 mil	.5 mil
Mask L_C	.4 mil	.4 mil

TABLE B-III DESIGN SPECIFICATIONS

The cells are designed to drive either a 4-pF or a 2-pF load under the conditions specified below:

V_{DD} 13.3 - 15.3 volts

V_{GG} 23.8 - 27.4 volts

V_T 3.5 - 4.5 volts

K' 1.8 - 2.2 for deep diffusion process

3 - 4 for shallow diffusion process

K' vs Temp $T^{-3/2}$

V_T vs. substrate bias $V_T + 1/2\ (VBS)^{1/2}$

Lateral diffusion 0.12 mil (deep diffusion)

0.05 mil (shallow diffusion)

Temp: -55 to +135°C

Mask alignment tolerance: 0.1 mil

(Resistance of p region)
R_{PN} 150 Ω per square

(Capacitance of p region)
C_{PN} 0.07 pF/mil^2

(Metal to thick oxide)
C_{MF} 0.02 pF/mil^2

(Metal to thin oxide)
C_{MG} 0.2 pF/mil^2

The process and environmental specification require the cells to perform over a wide range of K' values. Thus the extreme values of K' become

$$K'_{135} = K'_{min} \left(\frac{T_{135}}{T_{25}}\right)^{-3/2} = K'_{min} \left(\frac{408}{298}\right)^{-3/2} = .624\ K'_{min}$$

and

$$K'_{-25} = K'_{min} \left(\frac{T_{-55}}{T_{25}}\right)^{-3/2} = K_{max} \left(\frac{218}{298}\right) = 1.6\ K'_{max}$$

where

K'_{min} is the minimum value of K' at 25°C
K'_{max} is the maximum value of K' at 25°C

K'_{135} is the minimum value of K' at 135°C
and K_{-55} is the maximum value of K' at -55°C

Thus with shallow diffusion

$K'_{135} = 1.86$
and $K'_{-55} = 6.38$

with the deep diffusion

$K'_{135} = 1.12$
$K'_{-55} = 3.51$

Appendix C

CELL INDEX

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
2070-2080	2-Input NOR, 2pF	DS-1	CTF-1
2090-2100	2-Input NOR, with delay, 2pF	DS-3	CTF-1
2110-2120	3-Input NOR, 2pF	DS-5	CTF-1
2130-2140	3-Input NOR with delay, 2pF	DS-7	CTF-2
2150-2160	4-Input NOR, 2pF	DS-9	CTF-2
2190-2200	2-Input NAND, 2pF	DS-11	CTF-2, CTF-3
2210-2220	2-Input NAND with delay, 2pF	DS-13	CTF-3
2230-2240	3-Input AND NOR, 2pF	DS-15	CTF-3
2250-2260	3-Input AND NOR with delay, 2pF	DS-17	CTF-3, CTF-4
2270-2280	4-Input NAND OR, 2pF	DS-19	CTF-4
2290-2300	4-Input AND NOR, 2pF	DS-21	CTF-4
2310-2320	4-Input AND NOR with delay, 2pF	DS-23	CTF-5
2330-2340	3-Input OR NAND, 2pF	DS-25	CTF-5
2350-2360	3-Input Switch, 2pF (optional EXCLUSIVE OR)	DS-27	CTF-5, CTF-6
2370-2380	Dynamic Shift Register, 2pF, with 1/2 bit and 1 bit delay outputs	DS-29	CTF-6
2390-2400	Dynamic Shift Register, 2pF, 1 bit delay output, with set	DS-31	CTF-6
2410-2420	Dynamic Shift Register, 2pF, 1 bit delay output, with reset	DS-33	CTF-6, CTF-7

CELL INDEX (Continued)

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
2440	Static Register, 2pF, "1" output with set	DS-35	CTF-7
2460	Static Register, 2pF, "0" and "1" outputs	DS-37	CTF-7
2480	Static Register, 2pF, "0" and "1" outputs with reset	DS-39	CTF-7
2500	Static Register, 2pF, "0" and "1" outputs set and kill	DS-41	CTF-7
2520	Dual Sample Register, 2 pF, "0" and "1" outputs	DS-43	CTF-8
2560	Schmitt Trigger	DS-45	CTF-8
2580	Dynamic Shift Register, 2pF, 1 bit delay output.	DS-47	CTF-8
2600	Static Register, 2pF, "1" output	DS-49	CTF-8
2620	Static Register, 2pF, "1" output with reset	DS-51	CTF-8
2640	Static Register, 2pF, "0" and "1" outputs with set	DS-53	CTF-9
2660	Static Register, 2pF, "0" and "1" outputs with kill	DS-55	CTF-9
2680	Static Register, 2pF, "0" and "1" outputs, reset and kill	DS-57	CTF-9
2700	Binary, 2pF, "0", carry and carry not outputs	DS-59	CTF-9

CELL INDEX (Continued)

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
4010-4020	Inverter, 4pF	DS-61	CTF-10
4050-4060	Inverter with delay, 4pF	DS-63	CTF-10
4070-4080	2-Input NOR, 4pF	DS-65	CTF-10
4090-4100	2-Input NOR with delay, 4pF	DS-67	CTF-10, CTF-11
4110-4120	3-Input NOR, 4pF	DS-69	CTF-11
4130-4140	3-Input NOR with delay, 4pF	DS-71	CTF-11
4150-4160	4-Input NOR, 4pF	DS-73	CTF-12
4170-4180	4-Input NOR with delay, 4pF	DS-75	CTF-12
4190-4200	2-Input NAND, 4pF	DS-77	CTF-12, CTF-13
4210-4220	2-Input NAND with delay, 4pF	DS-79	CTF-13
4230-4240	3-Input AND NOR, 4pF	DS-81	CTF-13
4250-4260	3-Input AND NOR with delay, 4pF	DS-83	CTF-13, CTF-14
4350-4360	3-Input Switch, 4pF (optional EXCLUSIVE OR)	DS-85	CTF-14
4370-4380	Dynamic Shift Register, 4pF, with 1/2 bit and 1 bit delay outputs	DS-87	CTF-14
4390-4400	Dynamic Shift Register, 4pF, 1 bit delay output, with set	DS-89	CTF-14, CTF-15
4410-4420	Dynamic Shift Register, 4pF, 1 bit delay output, with reset	DS-91	CTF-15

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
4430	Static Register, 4pF, "1" output w/reset, w/o int. C.G.	DS-93	CTF-15
4440	Static Register, 4pF, "1" output with set	DS-95	CTF-15
4450	Static Register, 4pF, "0" and "1" outputs w/reset, w/o int. C.G.	DS-97	CTF-16
4460	Static Register, 4pF, "0" and "1" outputs	DS-99	CTF-16
4480	Static Register, 4pF, "0" and "1" outputs with reset	DS-101	CTF-16
4500	Static Register, 4pF, "0" and "1" outputs, set and kill	DS-103	CTF-16
4520	Dual Sample Register, 4pF, "0" and "1" outputs	DS-105	CTF-16
4530-4540	RS Flip-Flop, no delay, 4pF, "0" and "1" outputs	DS-107	CTF-17
4580	Dynamic Shift Register, 4pF, 1 bit delay output	DS-109	CTF-17
4600	Static Register, 4pF, "1" output	DS-111	CTF-17
4620	Static Register, 4pF, "1" output with reset	DS-113	CTF-17
4640	Static Register, 4pF, "0" and "1" outputs with set	DS-115	CTF-18
4660	Static Register, 4pF, "0" and "1" outputs with kill	DS-117	CTF-18
4680	Static Register, 4pF, "0" and "1" outputs, reset and kill	DS-119	CTF-18

CELL INDEX (Continued)

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
6000-6010	Protected Clock Gate	DS-121	CTF-19
6020-6030	Clock Gate	DS-123	CTF-19
6040	Killer, ϕ_2 controlled	DS-125	CTF-19
6050	Killer, signal controlled	DS-127	CTF-19
6060	DC Buffer, 25pF	DS-129	CTF-20
6070-6080	Precharge Buffer, 53pF	DS-131	CTF-20
6090-6100	Precharge Buffer, 78pF	DS-133	CTF-20
6110-6120	Precharge Buffer, 103pF	DS-135	CTF-20
6140	Static Register String Start	DS-137	CTF-21
6160	Static Register String Middle	DS-139	CTF-21
6180	Static Register String End	DS-141	CTF-21
6200	Dynamic Register String Start	DS-143	CTF-21
6220	Dynamic Register String Middle	DS-145	CTF-21
6240	Dynamic Register String End	DS-147	CTF-21
6250-6260	Inverter, 10pF	DS-149	CTF-21, CTF-22
6270	ϕ_n Clock Gate	DS-151	CTF-22
6280	ϕ_n Protected Clock Gate	DS-153	CTF-22

Cell No.	Cell Name	Pg. No. of Data Sheet (Sec. IV. B)	Pg. No. of Circuit Type File (Sec. IV. C)
7020	Tunnel end	DS-155/156	No Circuit Type File
7030	Tunnel end	DS-155/156	
7510	On-chip alignment pattern	DS-155/156	
8040	Thick-oxide test transistor	DS-157/158	
8070	ϕ_1, V_{DD} pad pattern	DS-159/160	
8080	ϕ_2, GND pad pattern	DS-161/162	
9034	Pad	DS-155/156	CTF-22
The following cells were added in January, 1969.			
2570	Schmitt Trigger, ϕ	DS-45/46	CTF-8
5020	Protective Diode	DS-120A/120B	CTF-18
5030-5040	2-Input NOR, 9 pF	DS-1200/120D	CTF-18
5090	Killer, ϕ controlled	DS-120E/120F	CTF-19
6290-6300	Precharge Buffer, 30 pF	DS-154A/154B	CTF-22
The following cell was added in June, 1969.			
2720	Dual Sample Register, 2 pF, "1" output	DS-60A/60R	CTF-9

APPROVAL

BANNING STANDARD CELL ENGINEERING NOTEBOOK

Design Techniques Branch

The information in this report has been reviewed for security classification. The report, in its entirety, has been determined to be unclassified and contains no information concerning Department of Defense or Atomic Energy Commission programs.

This document has also been reviewed and approved for technical accuracy.

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